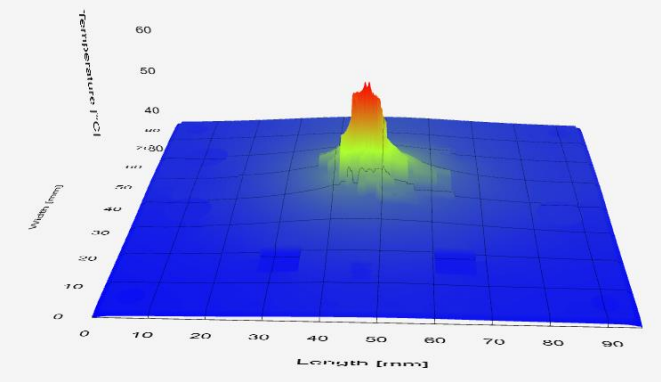

A STUDY ABOUT EVAL-LTM4703-AZ EVALUATION BOARD WITH TRM

Experiment and Simulation

ABSTRACT

Switching regulators are essential in modern power electronics, enabling efficient voltage conversion across various applications. However, their performance is closely tied to thermal management, as power dissipation during switching operations can lead to significant temperature rise, affecting efficiency, reliability, and longevity. This study focuses on the EVAL-LTM4703-AZ evaluation board, a high-efficiency, dual-channel µModule® regulator capable of delivering up to 12A. The compact design and high-power density of this regulator make it an ideal candidate for analyzing thermal challenges in switching regulators. By bridging theoretical modeling, experimental validation, and simulation, this work comprehensively assesses temperature rise and associated phenomena. Methods to calculate power losses, measure thermal profiles under operational stress, and simulate heat distribution using TRM software are presented. Additionally, voltage drops across parasitic resistances are quantified, highlighting their impact on system efficiency. The findings aim to aid engineers in optimizing thermal design in high-current switching regulators, balancing power density with thermal reliability

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A Study about EVAL-LTM4703-AZ with TRM

May, 2025

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I. Introduction

Switching regulators are essential in modern power electronics, enabling efficient voltage conversion across various applications, from portable devices to industrial systems. However, their performance is inherently tied to thermal management, as power dissipation during switching operations can lead to significant temperature rise, compromising efficiency, reliability, and longevity. Quantifying and mitigating these thermal effects is critical, particularly in high-current applications where voltage (IR) drops, and localized heating become pronounced. This paper focuses on the EVAL-LTM4703-AZ evaluation board, a high-efficiency, dual-channel µModule® regulator capable of delivering up to 12A [1]. Its compact design and high-power density make it an ideal candidate for analyzing thermal challenges in switching regulators.

This work bridges theoretical modeling, experimental validation, and simulation to comprehensively assess temperature rise and associated phenomena. We present methods to calculate power losses, measure thermal profiles under operational stress, and simulate heat distribution using TRM software [2]. Additionally, voltage drops across parasitic resistances are quantified, highlighting their impact on system efficiency. By correlating experimental data with simulation results, this study offers actionable insights for optimizing thermal design in high-current switching regulators. The findings aim to aid engineers in balancing power density with thermal reliability, a recurring challenge in advanced power systems.

II. Evaluation Board Details

The LTM®4703 is a high-efficiency, 12A step-down DC/DC µModule® regulator engineered to deliver precision power conversion in compact, space-constrained applications [3]. Encapsulated in a 6.25mm × 6.25mm × 5.07mm ball grid array (BGA) package, this fully integrated solution combines advanced power management capabilities with a robust 3V to 16V input voltage range and a configurable output voltage range of 0.3V to 6V. The output voltage is programmatically set via a single external resistor, ensuring design flexibility while maintaining ±1% output accuracy across line, load, and temperature variations.

A. 3D CAD View

Figure 1 and Figure 2 present a professional 3D visualization of PCB design. The top view shows the layout of key components, clearly marking the placement of the high frequency switching controller. The bottom view provides insight into the thermal management design, showcasing the thermally enhanced substrate that aids in heat dissipation. This visualization serves as a valuable tool for engineers to understand component arrangement and thermal design considerations.

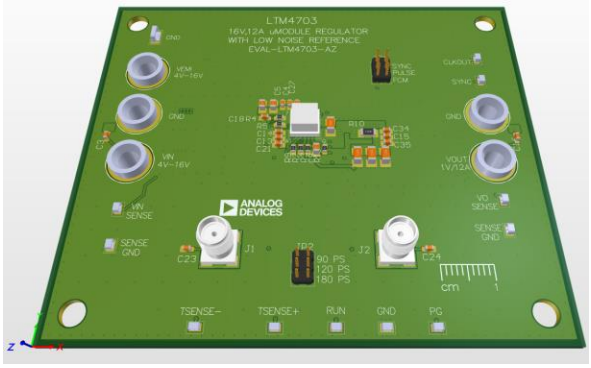


Figure 1 Top View 3D Visualization of Evaluation Board (EVAL-LTM4703-AZ)

Figure 2 Bottom View 3D Visualization of Evaluation Board (EVAL-LTM4703-AZ)

B. Key Technical Specifications and Integration

The device employs a synchronous buck topology with integrated critical components, including a high-frequency switching controller, low-loss N-channel power MOSFETs, and a shielded, high-current inductor, as illustrated in Figure 3. This monolithic integration eliminates the need for discrete magnetics and complex compensation networks, significantly reducing the total solution footprint and design iteration time. The architecture minimizes switching noise and ensures consistent output ripple performance, even under dynamic load conditions.

C. Simplified External Component Requirements

Design complexity is further reduced through the elimination of ancillary circuitry; only bulk input and output capacitors are required to stabilize the power delivery network (PDN). The input capacitor bank supports wide voltage transients and minimizes EMI, while the output capacitors ensure low impedance across the operating frequency range. This streamlined approach reduces bill-of-materials (BOM) count and enhances reliability in mission-critical systems.

D. Thermal and Performance Advantages

The BGA package LTM®4703 incorporates a thermally enhanced substrate with the following thermal characteristics from the [4]

TJMAX = 125°C, θJA = 19.6°C/W, θJCtop = 15.2°C/W, θJCbottom = 4.0°C/W.

“θ values are determined by simulation per JESD-51 conditions. θJA value is obtained with evaluation board”.

The device leverages a constant-frequency peak current-mode control scheme with optional spread-spectrum modulation, optimizing efficiency (up to 94% at full load) while mitigating electromagnetic interference (EMI).

E. Application Versatility

Ideal for high-density power systems in telecommunications infrastructure, data center ASIC/FPGA core supplies, and industrial automation, the LTM®4703 excels in environments demanding low noise, high power density, and rapid transient response. Its wide input range supports intermediate bus architectures (IBA) and direct operation from 12V/5V distribution rails.

F. Protection and Compliance Features

Integrated safeguards include overcurrent protection (OCP), overtemperature shutdown (OTSD), and input undervoltage lockout (UVLO), ensuring robust fault tolerance. Compliant with industrial temperature standards (-40°C to +125°C junction temperature), the µModule® adheres to stringent reliability requirements for aerospace, automotive, and industrial applications.

By consolidating power stage components, control logic, and thermal management into a single package, the LTM®4703 represents a paradigm shift in high-current DC/DC regulation, enabling engineers to achieve industry-leading performance with minimal layout and validation overhead.

The package includes the switching controller, the power MOSFETs, and an inductor as shown in Figure 3.

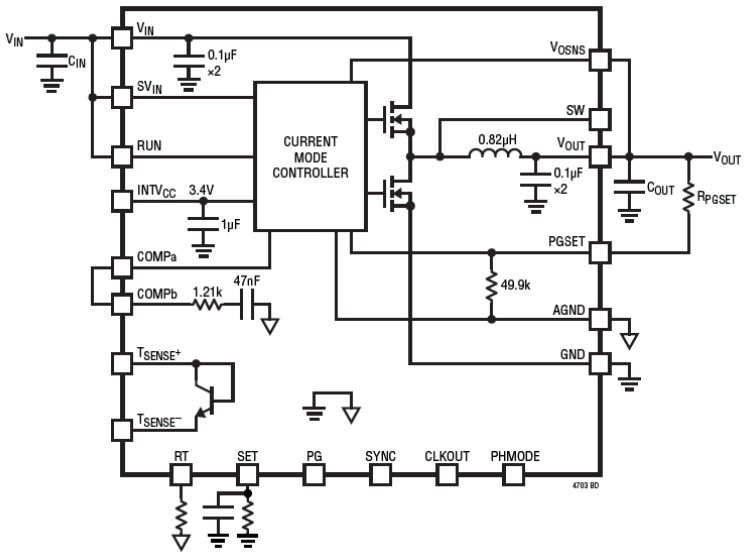


Figure 3 LTM4703 Block Diagram that shows the 0.82uH Inductor [4]

The inductor is strategically positioned on top of the component, as depicted in Figure 4, leveraging a 3D packaging approach to maximize power density and minimize the overall footprint of the solution. This innovative design integrates the inductor directly onto the substrate, reducing parasitic inductance and resistance while enhancing thermal performance. The proximity of the inductor to the power MOSFETs and controller minimizes loop area, which is critical for achieving low electromagnetic interference (EMI) and high efficiency in high frequency switching applications. This vertical integration approach is a hallmark of Analog Devices' µModule® technology, enabling a compact, high-performance power solution that simplifies PCB layout and reduces system-level design complexity.

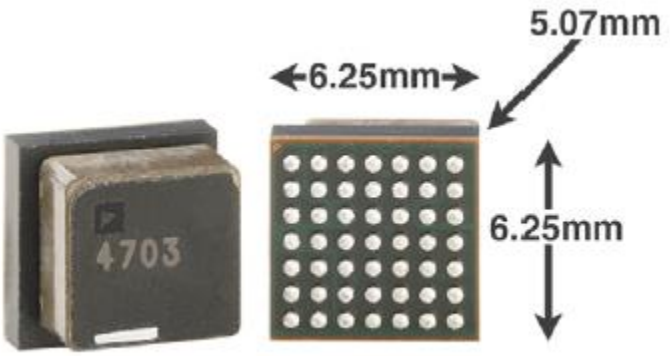


Figure 4 LMT4703 Component Image and dimensions [4]

G. Package Details and Mechanical Design

The LTM®4703 is housed in a 49-pin BGA package with dimensions of 6.25mm × 6.25mm × 5.07mm. The package is designed to provide robust mechanical stability and excellent thermal conductivity, ensuring reliable operation in demanding environments. The detailed mechanical specifications, including pad layout, solder ball configuration, and thermal performance metrics, are available in [4] and [5] .

The package features a low-profile design with a thermally enhanced substrate that facilitates efficient heat dissipation. The solder balls are arranged in a grid pattern to optimize electrical connectivity and mechanical strength, while the underfill material ensures long-term reliability under thermal cycling and mechanical stress. The package is also designed to accommodate automated assembly processes, making it suitable for high-volume manufacturing.

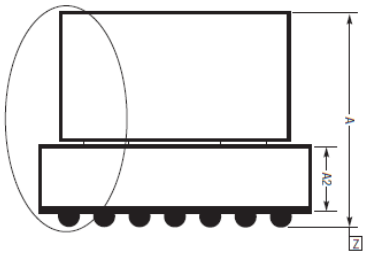


Figure 5 LMT4703 Block Diagram that shows the 0.82uH Inductor

H. Thermal Management and Reliability

The inductor's placement on top of the component, combined with the package's thermal design, ensures effective heat dissipation even under high load conditions. The thermal resistance (θJA) of the package is minimized using advanced materials and design techniques, enabling the LTM®4703 to deliver full-rated current without thermal derating. This is particularly important in applications where space constraints limit the use of external heat sinks or cooling solutions.

I. Electrical Performance and Layout Considerations

The integration of the inductor into the package reduces the need for external magnetics, simplifying the PCB layout and reducing the overall solution size. The package design minimizes parasitic inductance and resistance, which are critical for maintaining high efficiency and low noise in high frequency switching regulators. The close coupling of the inductor to the power stage also reduces switching losses and improves transient response, making the LTM®4703 ideal for applications requiring fast load-step performance.

J. Application-Specific Advantages

The compact form factor and high level of integration make the LTM®4703 particularly well-suited for space-constrained applications such as telecommunications infrastructure, data center equipment, and portable medical devices. The package's robust design ensures reliable operation in harsh environments, including those with high levels of vibration, shock, and temperature extremes.

By combining advanced packaging technology with high-performance power management, the LTM®4703 sets a new standard for compact, efficient, and reliable DC/DC conversion. The detailed package information provided in the datasheet allows engineers to fully leverage the benefits of this innovative design, ensuring optimal performance in their specific applications.

We will focus on the **Evaluation Board (EVAL-LTM4703-AZ)** provided by the manufacturer, which is designed to demonstrate the performance and capabilities of the LTM®4703 µModule® regulator [6]. The evaluation board will be configured to operate with an **output voltage of 1V** and an **output current of 12A**, delivering a total power output of 12W. The switching frequency (Fsw) will be set to **400 kHz**, a value chosen to balance efficiency, thermal performance, and component size. The input voltage will be supplied at **12V**, which is a common rail voltage in many industrial and telecommunications applications.

K. Efficiency Analysis

According to the LTM®4703 datasheet, the device exhibits an efficiency of approximately **86%** under the specified operating conditions (1V output, 12A load, and 12V input). This efficiency metric is critical for evaluating the thermal performance and power loss characteristics of the regulator. Figure 6 in the datasheet provides detailed efficiency curves for various output voltages and load conditions, enabling designers to assess the device's performance across a wide range of operating scenarios.

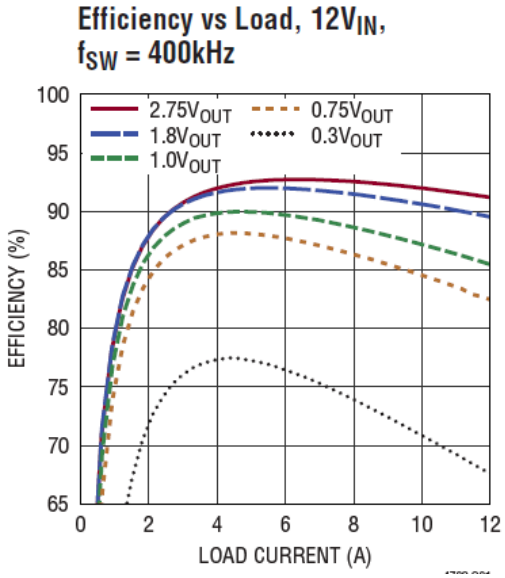


Figure 6 Efficiency vs Load performance characteristics [4]

At **12A load current**, the efficiency of 86% indicates that the power loss in the system is approximately **2W**. This power loss is primarily attributed to conduction losses in the power MOSFETs, switching losses, and core losses in the integrated inductor. The evaluation board's design ensures that these losses are effectively managed through optimized layout and thermal design.

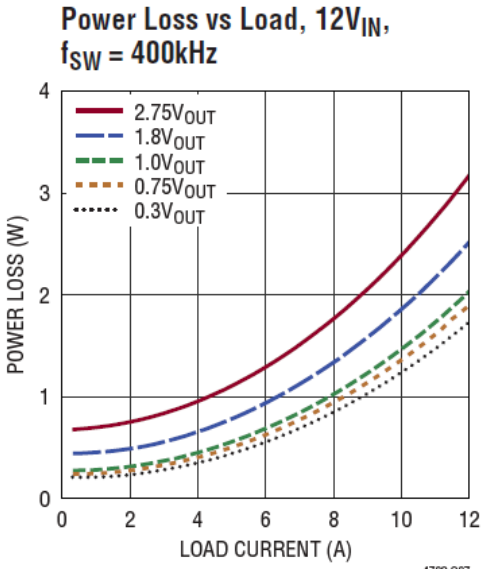


Figure 7 Power loss and Load relationship [4]

For the specified operating conditions—**12V input voltage**, and **12A load current**—the LTM®4703 µModule® regulator is expected to draw an **input current of approximately 1.2A**, as detailed in the datasheet and illustrated in Figure 7 . This current input value is derived from the power balance equation, accounting for the device's efficiency and the conversion of input power to output power.

L. Input Current

The current input of **1.2A** at **12V** as shown in Figure 8 reflects the regulator's ability to efficiently step down the voltage while delivering high output current. This low input current reduces stress on the input power source and minimizes losses in the input power distribution network (PDN). Additionally, the relatively low input current contributes to reduced thermal dissipation on the input side, further enhancing system reliability.

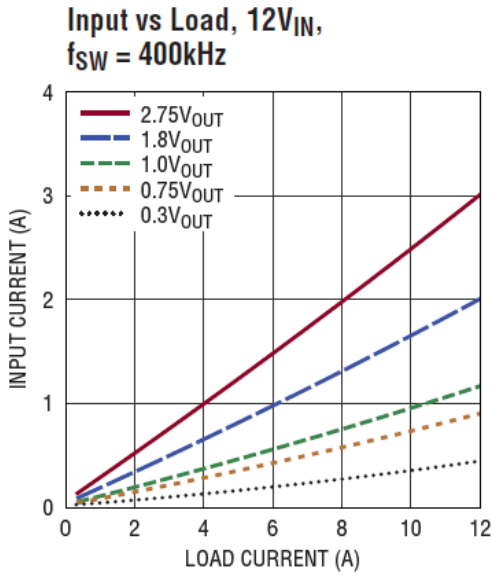


Figure 8 Input Current and Output Current relationship [4]

M. Design Files

The manufacturer provides a comprehensive suite of **design files** and documentation to facilitate the evaluation, prototyping, and integration of the **LTM®4703 µModule® regulator** into end applications. These resources include the **Bill of Materials (BOM)**, **Gerber files**, **Allegro PCB design files**, **schematic files**, and a detailed **user guide**. These materials are invaluable for engineers seeking to accelerate their design process and ensure optimal performance of the LTM®4703 in their systems.

Key Resources Provided by the Manufacturer

i. Schematic Files

The schematic files for the **EVAL-LTM4703-AZ** evaluation board are available at the following link: [7]

ii. User Guide

The user guide for the **EVAL-LTM4703-AZ** evaluation board is available at the following link: [1]

iii. Design Source

The complete set of design files, including the BOM, Gerber files, and Allegro PCB design files, is available in a compressed ZIP archive at the following link: [8]

N. Evaluation Board

Top Vie Photo image is show in Figure 9 that helps the reader to get familiar with the placement of the components and location of the device package and Input and Output connections.

Figure 9 EVAL-LTM4703-AZ Evaluation Board Picture [6]

Proper setup of the measurement is indicated in the Evaluation Board User Guide, from the top view of the image show in Figure 10, the Power supply input is show at the left of the Image, the user can setup an Ammeter in series with the Input Power Supply and a load must be connected at the Output, a DC Load is recommended to get more accurate information about the Output currents and or setup the Load as Constant current load and minimize the effect that can be encounter using resistor loads and the effect of the characteristics of the Resistor Value due to changes in the temperature increases. Sense Probes can be connected to the sense Test points shown in the image as sense.

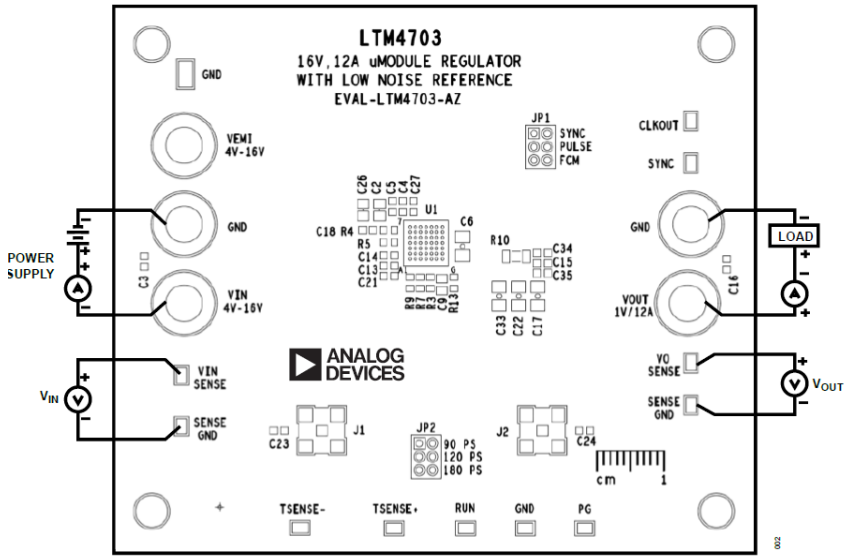


Figure 10 measurement equipment setup [6]

O. Evaluation Board Thermal Results

The datasheet shows a temperature plot with 12V input, 1V output at 12A without heatsink and no Airflow [3]. From Figure 11, It's important to notice the Infrared image Temperature scale from 25 to 110 and the difference in temperature at U1, it can be seen a difference of 2 Degrees from the lower/upper surface of the part. An assumption can be made due to the inductor being placed above the Regulator and expected more metal in the inductor that the IC can be considered for this assumption.

Figure 11 thermal image, 12Vin, 1Vout, 12A Output [4] [6].

An important consideration is the decreasing of the device performance at higher temperatures, Figure 12 shows the derating curve of the device [4]. If the device needs to operate at higher temperatures, from Figure 11, it can be easily calculated that the increase of temperature in the device is about 66-25 = 41. This is important information to consider in your final application.

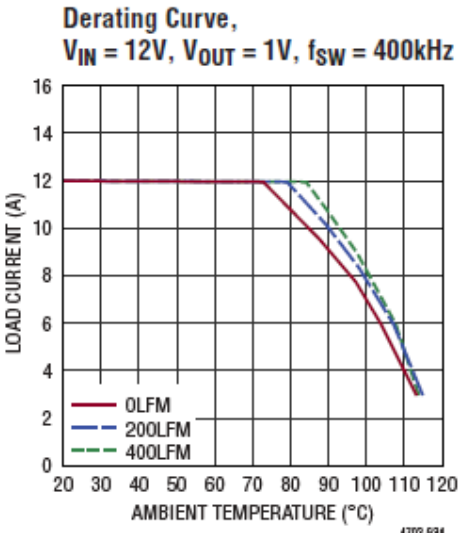


Figure 12, Derating Curve [4]

P. Circuit Design

The schematic of the evaluation board is shown in Figure 13 [7], the Input Power supply will be connected to E1 and E10, it can be seen that this is directly connected to the LTM4703 Device (U1) and the Output Voltage it does include a 0 ohm resistor in series (R10), the output Voltage or Load connections are to be made at E3 and E8.

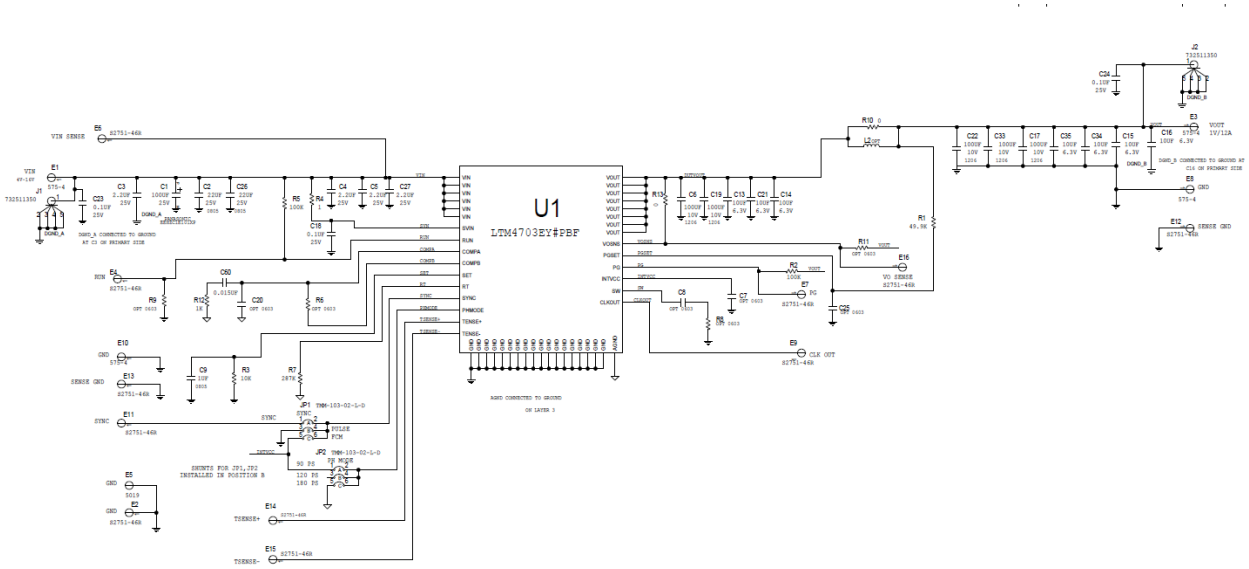


Figure 13 Evaluation Board circuit schematic [7]

Figure 14 shows some markups for the setup during the simulations and assignments for current setup and it's a representation of the Current Flow and indicates the main connectors for the setup of the Power supply and the Load.

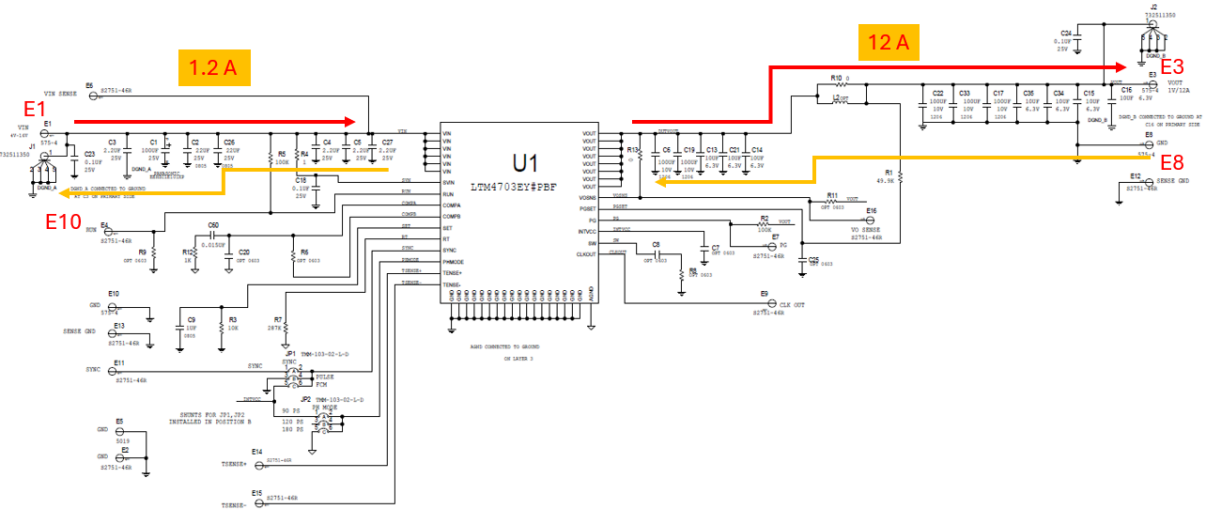


Figure 14 Example for Current Flow and instrument connections

III. PCB Preparation

A. PCB Stackup.

The PCB stackup drawing provided in the evaluation board documentation lacks clarity regarding the dielectric thickness of each layer. The documentation only includes the total thickness of the board and the number of layers, which is insufficient for accurate simulation modeling. Detailed stackup information is essential for the proper setup of the simulation model. Figure 15 illustrates the supplied stackup in the evaluation board documentation [8].

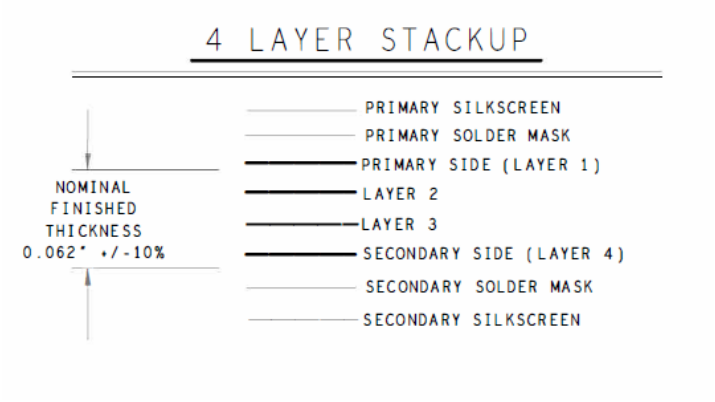


Figure 15 stackup drawing supplied in the evaluation board documentation

B. PCB Materials

The fabrication drawing provides some information about the material, but the thickness of each layer is not specified. The only available data is the material family, which can sometimes be helpful, but does not provide the material thickness. Knowing the thickness of the conductor layers is also important; in certain applications, a difference of ½ oz can be significant. Figure 16 shows the material specifications provided in the documentation.

SPECIFICATIONS:

MATERIALS:	ALL LAMINATES AND BONDING MATERIALS SHOULD BE SELECTED FROM IPC-4101 OR IPC-4103, MINIMUM Tg>170degC, Td>300degC, U.L. RATING OF 94 V-0
MATERIAL FAMILY:	FR406
CLADDING:	EXTERNAL LAYERS 1 OZ. COPPER, OVERPLATE TO 2 OZ. INTERNAL LAYERS 2 OZ. COPPER.

Figure 16 material specifications from evaluation board documentation

We created a non-professional micro-section on the evaluation board. Fortunately, the board includes copper extending to its edges. An examination of the PCB design in the CAD tool was necessary to identify areas suitable for sectioning. Some material must be removed to visualize the location of the copper layer relative to other layers.

By establishing a simple relation based on the total thickness of the board (1.6 mm), all other dimensions can be extrapolated using a linear relation and measured values averaged. Figure 17 illustrates the cross-sectional view of the board, where all four layers are visible.

Figure 17 cross sectional view of PCB

From the evaluation board, a cross-sectional cut and measurements was conducted to estimate the following stackup from the actual board. Figure 18 and Figure 19 display the calculated values from the section view. It can be inferred that the dielectric layer used between layer 1 and 2 is approximately 10 mils. Further analysis can be performed by reviewing the material datasheets and constructions for the material shown in the fabrication drawing.

#	Name	Material	Type	Weight	Thickness
	Top Overlay		Overlay		
	Top Solder	Solder Resist	Solder Mask		0.4mil
1	TOP		Signal	2oz	3.2mil
	Dielectric 1	FR-4	Prepreg		9mil
2	LAYER2		Signal	2oz	2.8mil
	Dielectric2	FR-4	Core		31mil
3	LAYER3		Signal	2oz	2.8mil
	Dielectric3	FR-4	Prepreg		9mil
4	BOTTOM		Signal	2oz	3.2mil
	Bottom Solder	Solder Resist	Solder Mask		0.4mil
	Bottom Overlay		Overlay		

Figure 18 measured values from the cross sectional cut (mils)

#	Name	Material	Type	Weight	Thickness
	Top Overlay		Overlay		
	Top Solder	Solder Resist	Solder Mask		0.01016mm
1	TOP		Signal	2oz	0.08128mm
	Dielectric 1	FR-4	Prepreg		0.2286mm
2	LAYER2		Signal	2oz	0.07112mm
	Dielectric2	FR-4	Core		0.7874mm
3	LAYER3		Signal	2oz	0.07112mm
	Dielectric3	FR-4	Prepreg		0.2286mm
4	BOTTOM		Signal	2oz	0.08128mm
	Bottom Solder	Solder Resist	Solder Mask		0.01016mm
	Bottom Overlay		Overlay		

Figure 19 measured values from the cross sectional cut (mm)

C. PCB Layers

The provided Gerber files include critical information on the board's dimensions and construction, along with the required details for its fabrication and assembly. Figure 20 displays all the supplied Gerber files within a CAM editor.

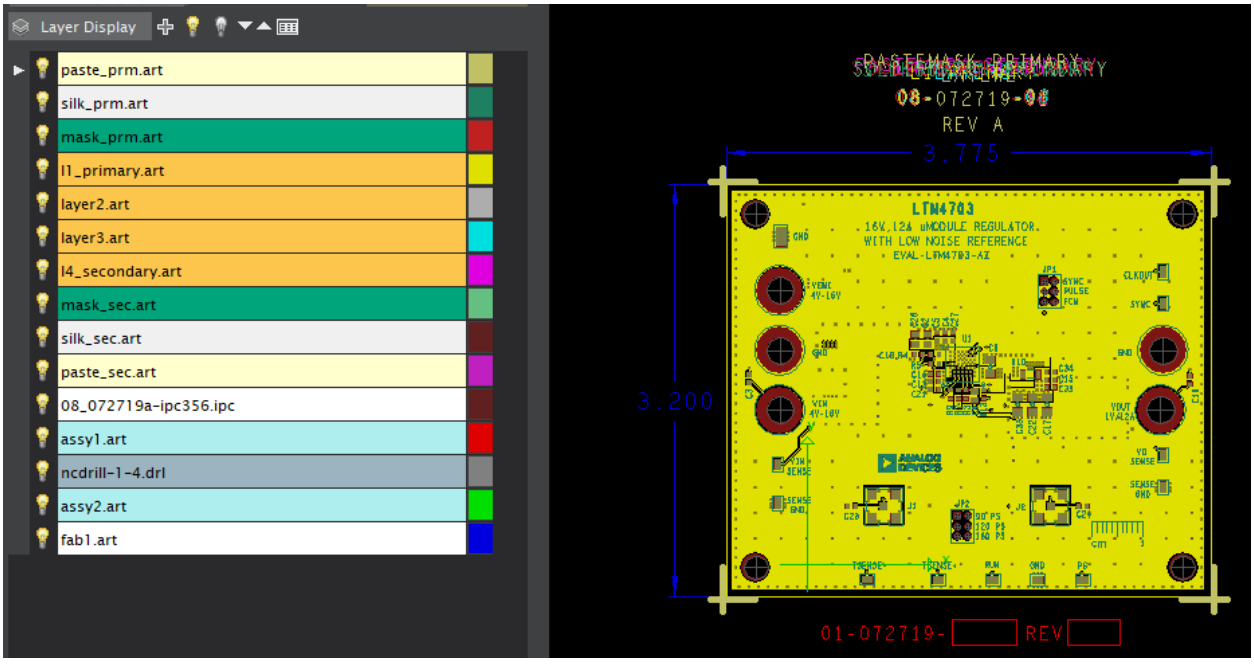


Figure 20 Supplied Gerber File [8]

The PCB stack-up consists of four electrical layers. The usage and net names for each layer are detailed below.

Top Layer: The top layer accommodates most of the main circuitry and includes small copper planes for the primary power path. Decoupling capacitors are placed on the side of the board, and this layer is also flooded with ground.

Layer 2: Layer 2 serves as a dedicated ground plane.

Layer 3: Layer 3 is designated for certain signals and the main input and output current paths. This layer is also flooded with ground.

Bottom Layer: The bottom layer is utilized for small power planes near the DUT (Device Under Test) and is similarly flooded with ground.

As illustrated, the four layers incorporate ground planes., Figure 21 presents each layer separately.

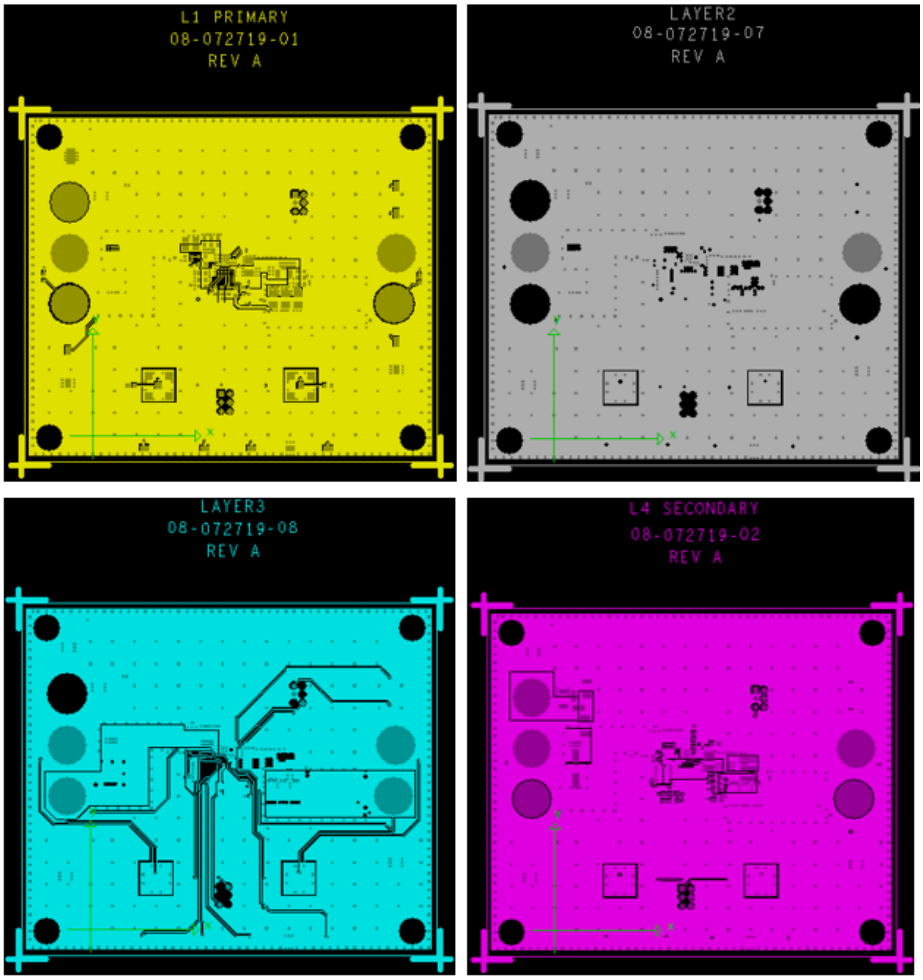


Figure 21 Electrical (Metallic) Layers

D. Simulation Software TRM by ADAM Research

A data sheet can neither reproduce nor predict the temperature of a user's application or board. TRM is calculating the realistic temperature field on a user application PCB. The block diagram merely shows an overview of the thermal path, whereby the lower right thermal resistance value depends on the specific layout. θ_{JA} is the condensed result of all the heat shoveling in the assembly and into the ambient air. Data sheet values θ_{JA} should merely be used to compare to vendors and never be used as an input value for simulation. In contrast θJCtop and θJCbottom are package specific internal thermal resistances which connect internal thermal nodes and could be used in a simulation if the junction temperature were of interest. However, in our case we measure the surface temperature and therefore rely on empirical thermal conductivity value.

From Package details from datasheet [4]*: page 2.*

θJA = 19.6°C/W,

θJCtop = 15.2°C/W,

θJCbottom = 4.0°C/W,

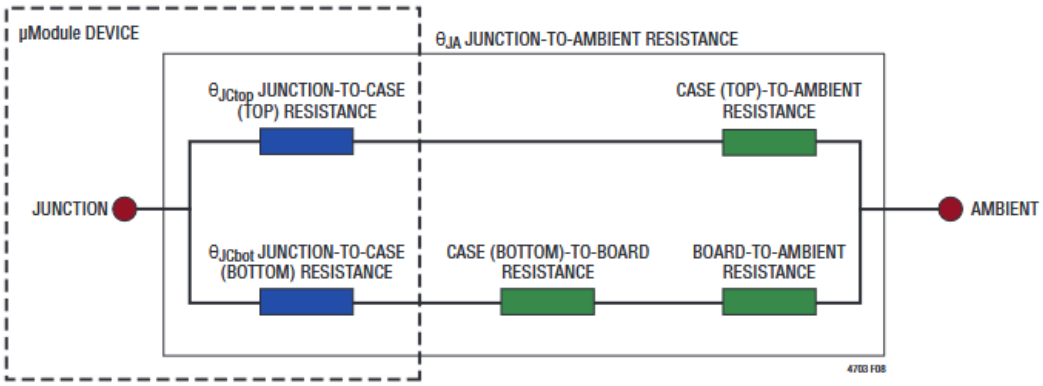


Figure 22 Thermal Coefficients from Datasheet [4].

The TRM software by ADAM Research combines both electrical and thermal analysis capabilities into a single, user-friendly package, offering a comprehensive solution for PCB designers and engineers [2]. Here's an overview of its electrical and thermal capabilities, along with the advantages of having them integrated:

Electrical Capabilities

Current Density Analysis: Provides detailed maps of current density to identify bottlenecks and areas of high current concentration.

Potential Drop Mapping: Offers precise maps of potential and potential drops across the PCB.

DC and Transient Simulations: Supports steady-state and transient simulations for accurate electrical performance predictions.

Inductance Matrix: Calculates self and mutual inductance for advanced circuit analysis.

Thermal Capabilities

Joule Heating Analysis: Calculates trace temperatures caused by current flow (Joule heating) and board heating from components.

High-Resolution Thermal Imaging: Generates virtual thermograms with high resolution for every layer of PCB.

Environmental Factors: Accounts for ambient temperature, convection, air speed, vacuum conditions, and wall temperature.

Transient Thermal Simulations: Allows for virtual thermal coupling and time-based temperature recording.

Advantages of an All-in-One Package

Integrated Analysis: Combines electrical and thermal simulations, enabling a holistic approach to PCB design and risk management.

Ease of Use: Designed for PCB designers and engineers without requiring expertise in numerical methods or CAD systems.

Cost-Effective: Eliminates the need for multiple software tools, reducing costs and streamlining workflows.

Enhanced Accuracy: Provides precise results by considering both electrical and thermal interactions, ensuring reliable PCB performance.

Flexible Input Formats: Supports various file formats like Gerber and Excellon, making it compatible with multiple layout systems and CAD tools.

This all-in-one approach simplifies the design process, reduces errors, and ensures that both electrical and thermal aspects are optimized for robust PCB performance. You can explore more details about TRM [2].

E. TRM Setup

The manufacturer provided the original CAD data, with the design available in Allegro format and Gerber files [8]. TRM supports Gerber files and includes a plugin for Cadence and other CAD vendors. The following models and calculations were done with release TRM3.9.

A test conversion was conducted to Altium Designer, and PCB libraries were updated to include more detailed component information, as shown in Figure 1, 3D bodies were added to the footprints. The Altium conversion requires adjustments to some parameters and rules to ensure proper connections of copper planes. After completing this process, it is recommended to create Gerber files from the conversion and compare each layer in the Gerber format.

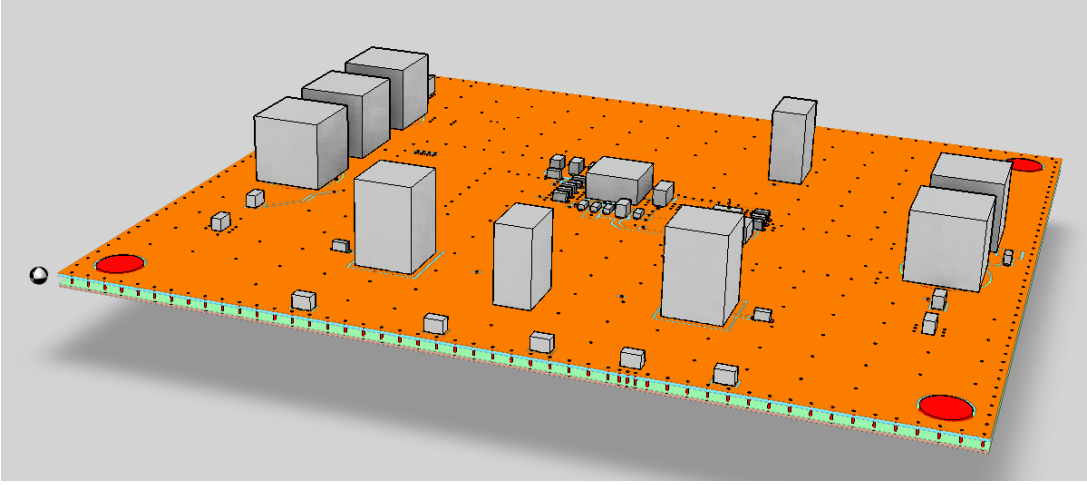


Figure 23 TRM 3D View of PCB

i. TRM Stackup

This section defines the stackup and materials, specifying the Conductor and Dielectric materials. Depending on the PCB construction materials, TRM provides a range of predefined material properties for further exploration. It is also possible to create own materials and to store them in a library.

	Level	Name	Type	File	View	FR4 white	Thick (um)	Conductor	Dielectric	Expose	Color
+ x	1	TOP	ger	TRM_1_TOP.art	View	☑	81	Cu$TRM	FR4$TRM	Expose	
+ x	2	Pre2	pre		View	☑	228	Cu$TRM	FR4$TRM		
+ x	3	LAYER2	ger	TRM_2_LAYER2.art	View	☑	71	Cu$TRM	FR4$TRM	Expose	
+ x	4	Pre3	pre		View	☑	787	Cu$TRM	FR4$TRM		
+ x	5	LAYER3	ger	TRM_3_LAYER3.art	View	☑	71	Cu$TRM	FR4$TRM	Expose	
+ x	6	Pre4	pre		View	☑	80	Cu$TRM	FR4$TRM		
+ x	7	BOTTOM	ger	TRM_4_BOTTOM.art	View	☑	71	Cu$TRM	FR4$TRM	Expose	

Figure 24, TRM Stackup setup (Allegro Design)

	Level	Name	Type	File	View	FR4 white	Thick (um)	Conductor	Dielectric	Expose	Color
+ x	1	Top Layer	ger	08_072719a.GTL	View	☑	81	Cu$TRM	FR4$TRM	Expose	
+ x	2	Dielectric	pre		View	☑	228	Cu$TRM	FR4$TRM		
+ x	3	Mid Layer 1	ger	08_072719a.G1	View	☑	71	Cu$TRM	FR4$TRM	Expose	
+ x	4	Dielectric	pre		View	☑	787	Cu$TRM	FR4$TRM		
+ x	5	Mid Layer 2	ger	08_072719a.G2	View	☑	71	Cu$TRM	FR4$TRM	Expose	
+ x	6	Dielectric	pre		View	☑	228	Cu$TRM	FR4$TRM		
+ x	7	Bottom Layer	ger	08_072719a.GBL	View	☑	81	Cu$TRM	FR4$TRM	Expose	

Figure 25 TRM Stackup setup (Altium Conversion)

The TRM [Prepare] Options display provides details about the resolution and relevant information regarding the board. During the import of design data, the only configuration required is the resolution. This factor is also crucial when conducting electrical and thermal simulations within TRM. For more comprehensive information, please refer to the TRM Manual.

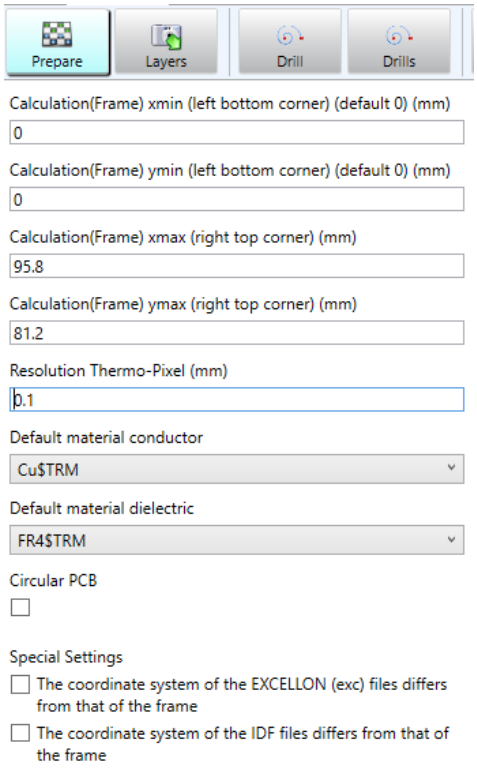


Figure 26 TRM Preparation Setup

ii. TRM Drill Files

Details about import holes or drilling can be found in the [Drill] menu, where adjustments to the original design can also be made if necessary. The TRM software allows users to set up various via span options, including blind, buried vias and backdrills, as well as specify the plating material and thickness. Additional experiments can be conducted using the software's features.

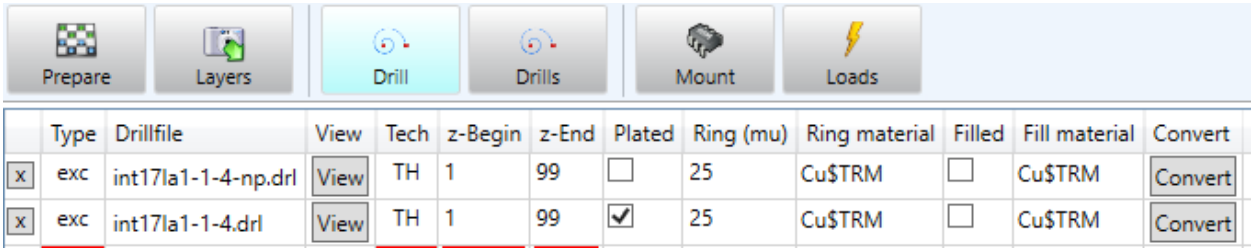


Figure 27 TRM Drill setup

iii. TRM Loads

Most of the detailed configuration occurs in the [Loads] menu within TRM (Figure 28) where information regarding components, nets, pins, materials, watts, amperes, and other relevant details are established. The Ampere Values are the quantity that was measured with the Amp Meter or the one provided or controlled by the DC Load.

	Index	Name	PosX (mm)	PosY (mm)	DimX (mm)	DimY (mm)	Height (mm)	Begin	End	Material	Form	K/W-board	K/W-air	Watt	Celsius	Ampere
+ X	68	U1	43.611	42.722	6.25	6.25	3.1	0	0	Comp_diel_loc$TRM	r	-1	-1	0.32		
+ X	112	DUTVOUT~R10-1	58.698	43.815	0.833	-1	2	1	1	Cu$TRM	c	-1	-1			-1
+ X	114	DUTVOUT~U1-A1	44.336	43.447	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			0.125
+ X	115	DUTVOUT~U1-A2	44.336	44.247	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			0.125
+ X	116	DUTVOUT~U1-A3	44.336	45.047	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			0.125
+ X	117	DUTVOUT~U1-B3	45.136	45.047	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			0.125
+ X	118	DUTVOUT~U1-F3	48.336	45.047	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			0.125
+ X	119	DUTVOUT~U1-G1	49.136	43.447	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			0.125
+ X	120	DUTVOUT~U1-G2	49.136	44.247	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			0.125
+ X	121	DUTVOUT~U1-G3	49.136	45.047	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			0.125

Figure 28 TRM Load Table

iv. TRM Environment

The [Test] Options display various test conditions and environmental setups for simulations. One of the key factors is the Total Heat Transfer coefficient, which can significantly impact results based on different power conditions, layers, and board sizes.

TRM also offers an advanced heat transfer setup and specialized configurations for vacuum conditions.

It is essential to evaluate these conditions and validate them with an initial simulation to account for the power dissipated by devices or copper. Airflow can also be factored into the evaluation.

The TRM environment allows users to configure various thermal and electrical parameters to optimize their simulations. One notable feature is the ability to set boundary conditions and define material properties, which can significantly influence the accuracy of the results. Furthermore, TRM includes options for transient simulations.

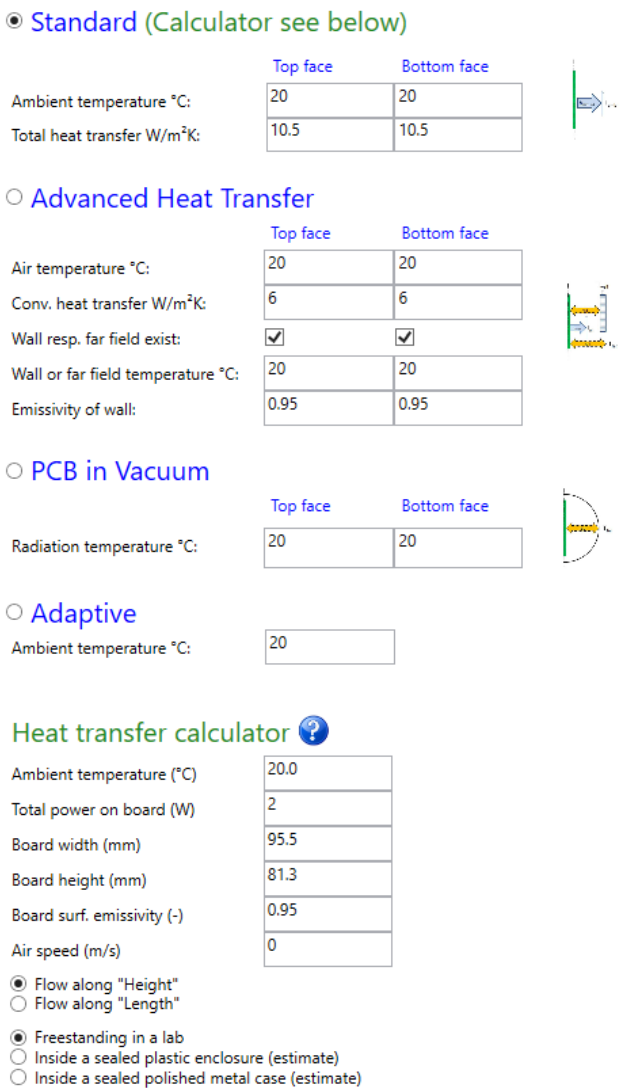


Figure 29 TRM Test Setup options

v. TRM Calculate

The [Calculation] menu offers useful options. You can enable the Current checkbox in “What to Calculate?” to check Voltage drop or Joule Heating in copper traces. The Temperature checkbox in “What to Calculate?” will Calculate the Temperature including Trace Heating and Component Heating.

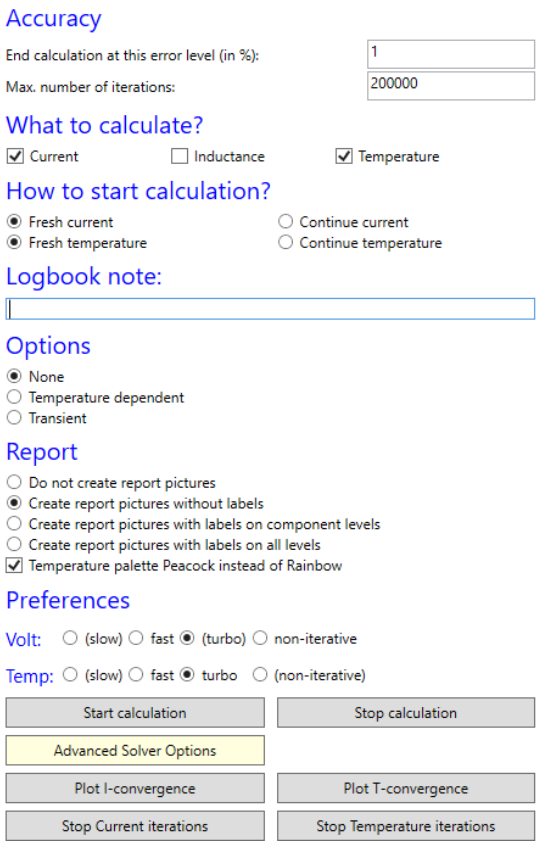


Figure 30 Calculation

For enhanced precision, TRM supports the implementation of temperature-dependent properties, ensuring that the simulations reflect real-world conditions more accurately. Users can visualize the impact of thermal expansion and contraction on the components, thereby gaining insight into potential issues that may arise during operation.

Many Options are available to configure and control the simulation, such as adjusting the power dissipation rates, specifying ambient temperature, and incorporating airflow effects. With these tools, engineers can perform comprehensive analyses and make informed decisions to improve the reliability and performance of their designs.

TRM also provides features to enable temperature dependency and transient simulations.

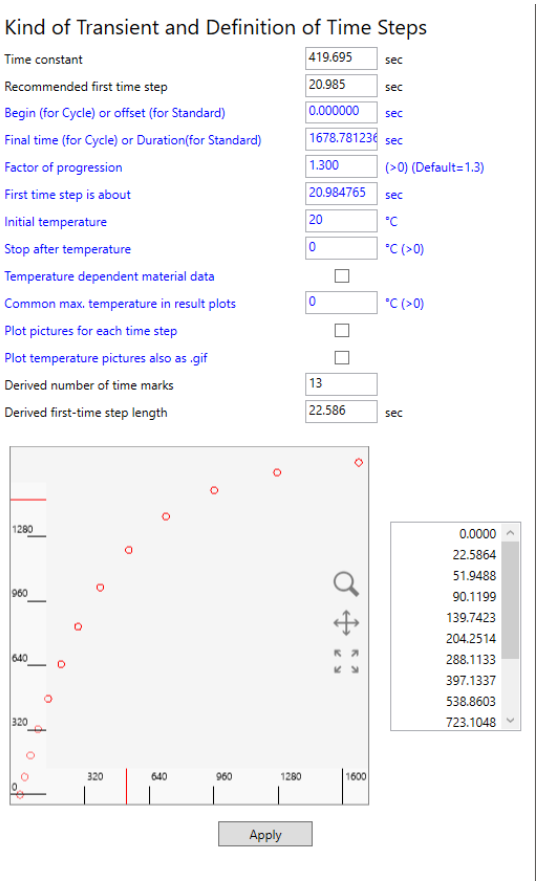


Figure 31 Transient Simulation and setup

vi. TRM Results

TRM provides various ways to visualize temperature, voltage, current density, thermal conductivity, electrical conductivity, and heat flux vector. Each variable can be visualized for every layer in the stack-up, as outlined in the TRM user manual.

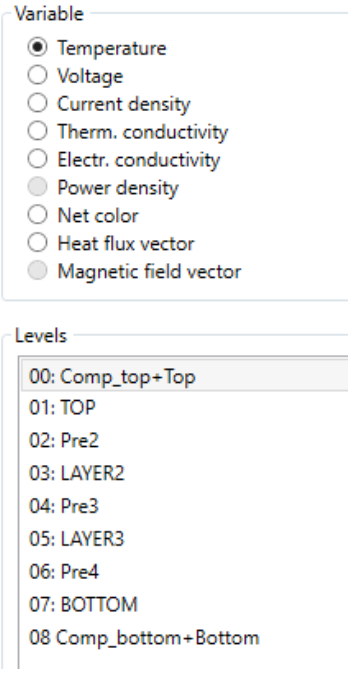


Figure 32 Simulation Results

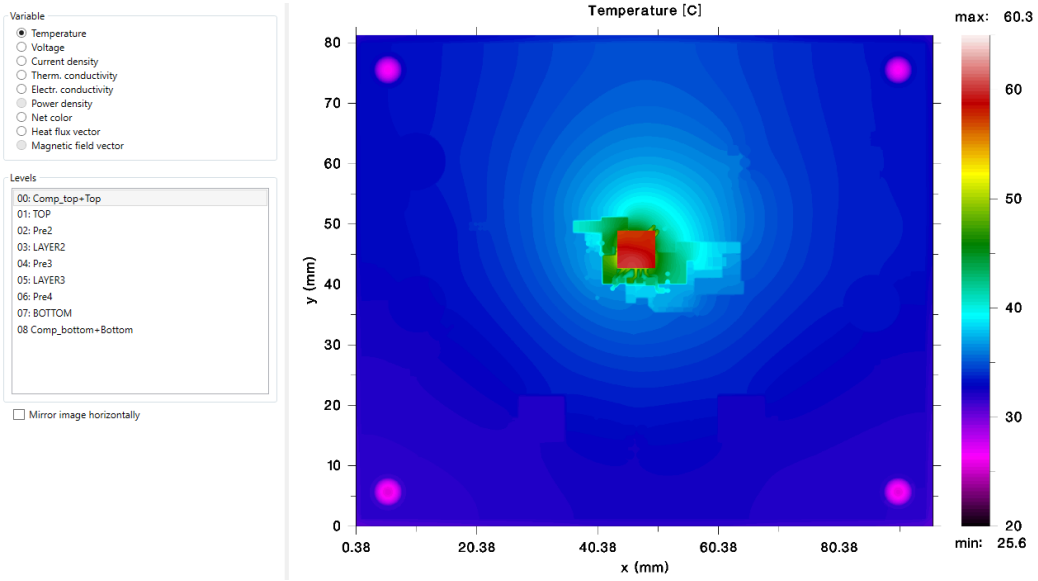


Figure 33 Temperature Plots

IV. Measurements

A. Bench Setup:

Voltage Connections: The wire was soldered to exposed pads or SMT leads on components. Figure 34 shows the connection points and wires soldered to the pad connections. These wires will connect the Voltage Meter to measure voltage differences between the points.

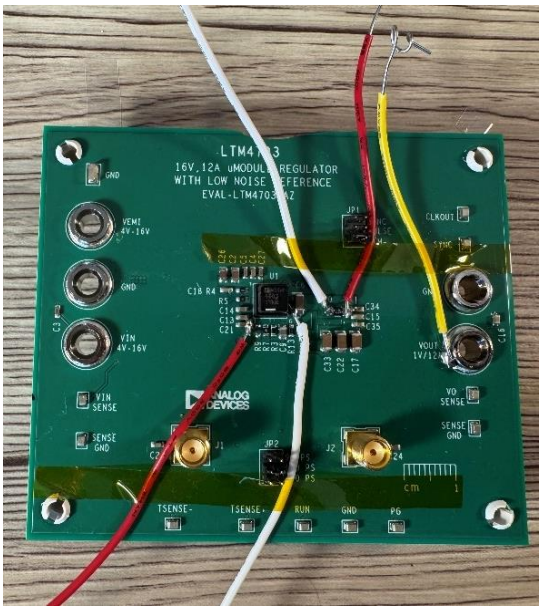


Figure 34 Voltage Probe connections for V1, V2, V3, V4 and V5

Thermocouples: Figure 35 shows thermocouple locations positioned near the component surfaces or PCB, secured with silicon tape for accurate measurements and stable contact.

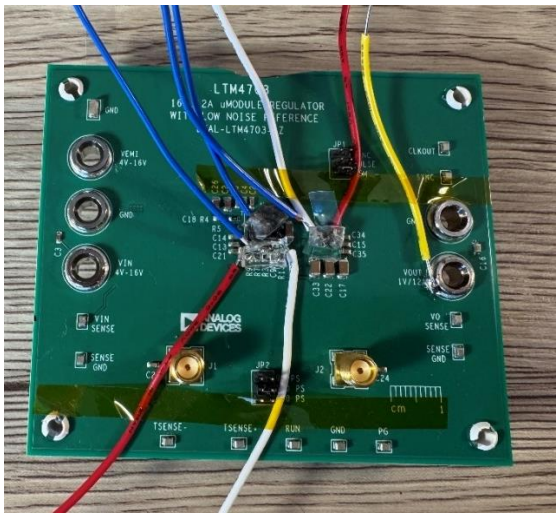


Figure 35 Thermocouple locations for T2, T3 and T4

Figure 36 and Figure 37 show how the instruments were connected to the board. The setup was not ideal or in a temperature-controlled room, but airflow control and minimizing light and human interaction were prioritized. Measurements were taken every 4 minutes for different current outputs, which is adequate for engineering research and comparisons with high confidence.

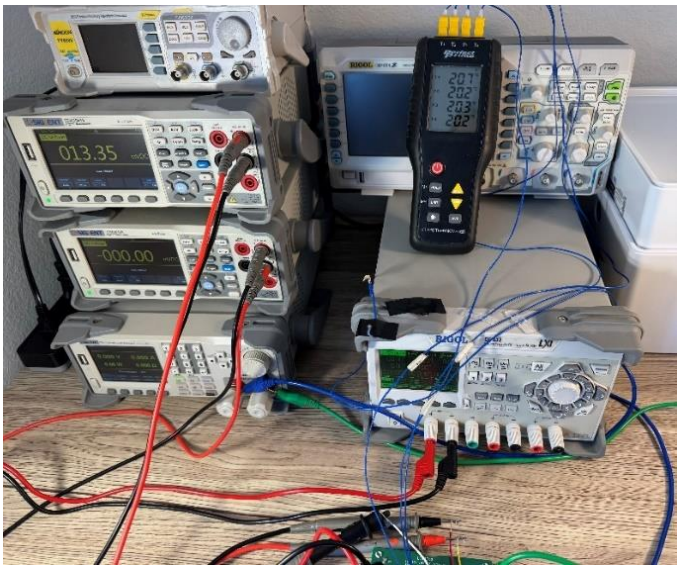


Figure 36 Instruments connections

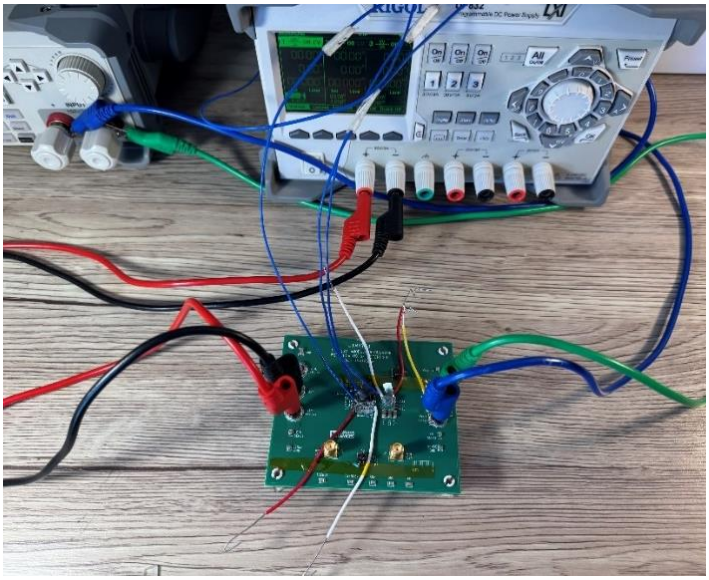


Figure 37 Input Voltage, DC Load, Voltage Probes and Thermocouple Locations on PCB.

B. Instrumentation used:

PerfectPrime, TC9815 4 Channels Thermocouple Thermometer

The PerfectPrime TC9815 is a high-precision, 4-channel thermocouple thermometer designed for multi-point temperature monitoring in industrial, laboratory, and commercial settings. It supports multiple thermocouple types (K, J, T, E, N, R, S) and features a large backlit display, data logging, and user-friendly controls. With its robust design and high accuracy (±0.3%), the TC9815 is ideal for applications such as industrial process monitoring, laboratory research, food safety, and environmental testing. Its ability to simultaneously monitor four temperature points makes it a versatile and reliable tool for demanding temperature measurement tasks.

Figure 38 PerfectPrime, TC9815

Sigilent, SDM3045X 4 1/2 Digits Dual-Display Digital Multimeter

The Siglent SDM3045X is a high-performance 4½-digit digital multimeter (DMM) featuring a dual-display for simultaneous measurement of two parameters. It offers precision voltage, current, resistance, and frequency measurements, with a 0.015% basic DC voltage accuracy. Equipped with advanced features like data logging, USB connectivity, and a clear LCD screen, the SDM3045X is ideal for laboratory, educational, and industrial applications requiring reliable and accurate measurements. Its robust design and user-friendly interface make it a versatile tool for professionals and enthusiasts alike.

Figure 39 Sigilent, SDM3045X

Sigilent, SDL1020X-E DC Electronic Load

The Siglent SDL1020X-E is a high-performance DC electronic load designed for testing and evaluating power sources such as batteries, power supplies, and fuel cells. With a power range of up to 200W and current up to 30A, it offers precise and dynamic loading capabilities. Key features include multiple operating modes (CC, CV, CR, CP), a 4.3-inch color display, and USB/LAN connectivity for remote control and data logging. Ideal for R&D, manufacturing, and quality assurance, the SDL1020X-E combines reliability, versatility, and ease of use for demanding power testing applications.

Figure 40 Sigilent, SDL1020X-E DC Electronic Load

Rigol, DP832 DC Power Supply

The Rigol DP832 is a versatile, triple-output programmable DC power supply designed for precision testing and development. It features two 30V/3A channels and one 5V/3A channel, offering a wide range of voltage and current outputs. With high resolution (1mV/1mA), intuitive controls, and advanced features like sequence and modulation modes, the DP832 is ideal for R&D, education, and industrial applications. Its robust design, coupled with USB, LAN, and GPIB connectivity, ensures reliable performance and seamless integration into automated test systems.

Figure 41 Rigol, DP832 DC Power Supply

C. Measured Data:

i. Power supply and Voltage connections

A voltage of +12V is applied to between E1 and E10. A DC load is connected between terminals E3 and E8. The Current on the load is controlled by the DC load and Measurements of the Current and Power consumption are provided by the Power supply and the DC Load.

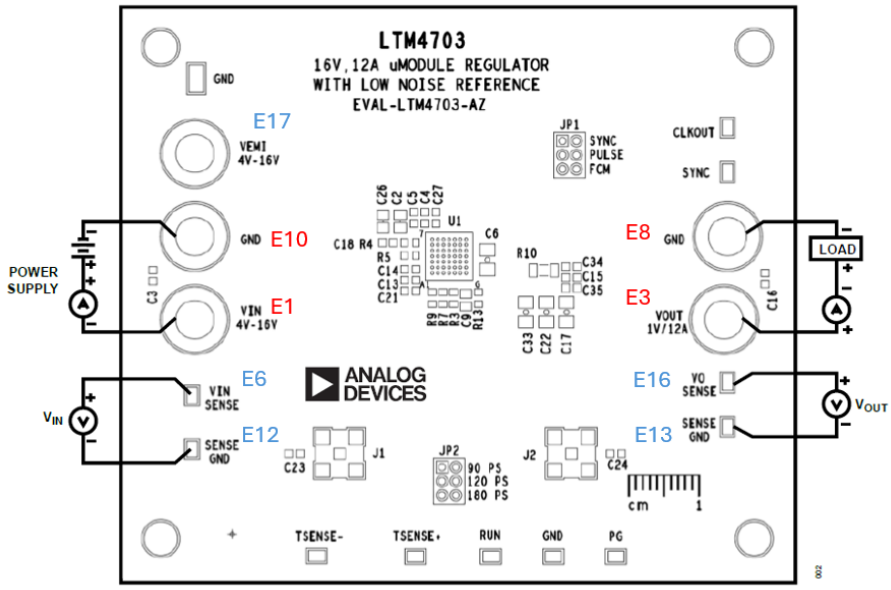


Figure 42 Power supply and DC load connection [6]

ii. Current and Power Measurements

A +12V input voltage is applied, with the output current set by the DL Load and controlled by the instrument. Power input comes from the power supply, while output power is provided by the DC Load, excluding resistive load consumption. Measurements are taken after 3 to 5 minutes to allow the evaluation board to reach a stable temperature.

Iout (A)	Iin (A)	Pout (W)	Pin (W)
1	0.11	1.00	1.32
2	0.19	2.00	2.28
3	0.28	3.00	3.36
4	0.37	4.00	4.44
5	0.46	5.00	5.52
6	0.56	6.00	6.72
7	0.66	7.00	7.92
8	0.76	8.00	9.12
9	0.86	9.00	10.32
10	0.96	10.00	11.52
11	1.07	11.00	12.84
12	1.17	12.00	14.04

Table 1 input and output Current and Power measurments

Figure 43 shows that the difference between power input and output begins to increase after 5 Amps of current output. Power loss is calculated as the difference between power output and power input.

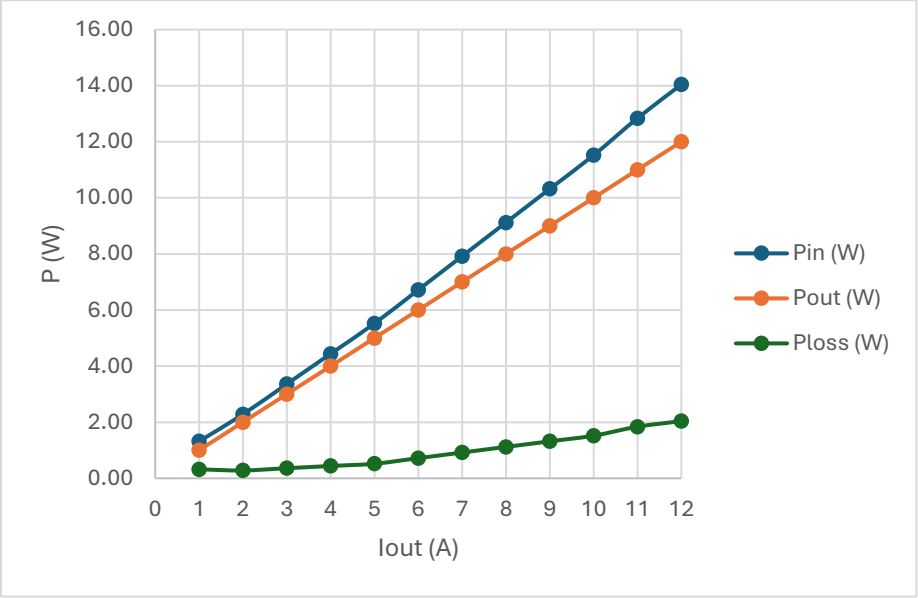


Figure 43, Power Measurements at different current outputs

iii. Effects on Power Input for different Current Output

As illustrated in Figure 44 and detailed in Table 1, the graphical representation of Iin demonstrates some degree of linearity. This indicates a direct correlation between the currents when the input and output voltages are held constant.

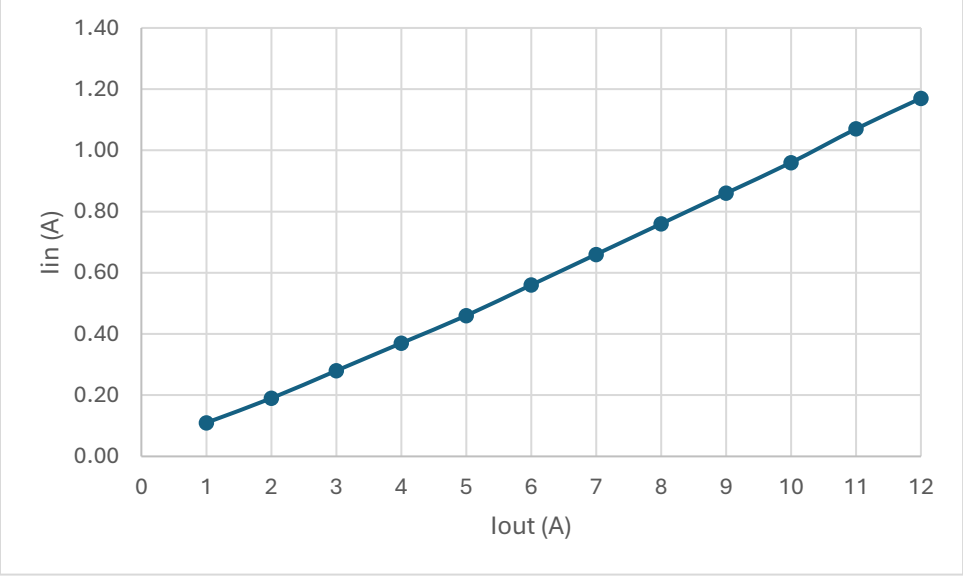


Figure 44 Relation between Iout and Iin

Table 1 provides a graphical representation of the power input, as shown in Figure 45, This is due to the linear relationship between the currents and the fixed voltages.

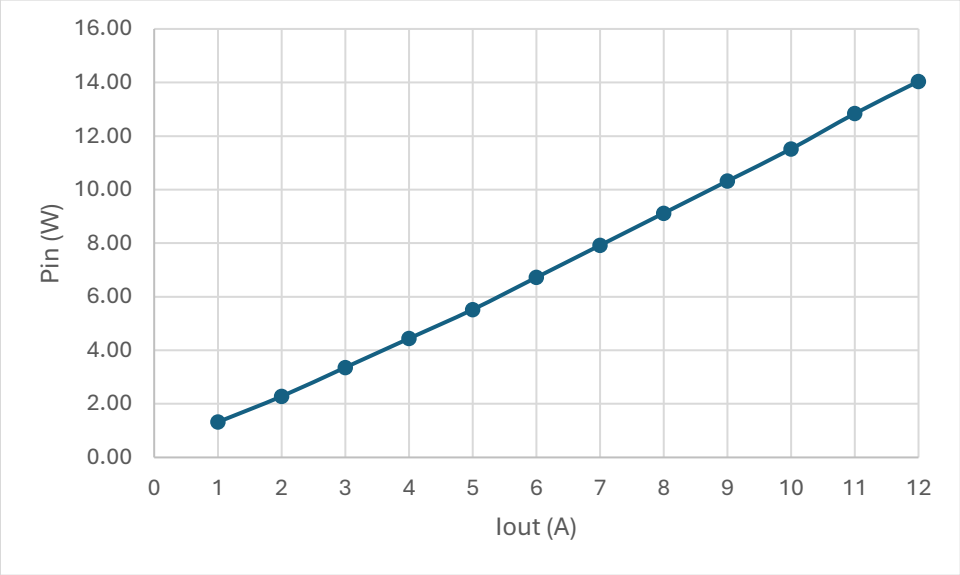


Figure 45 Relation between Power Input and Current Output

iv. Voltage measurements

Potential difference measurements were taken at various points on the evaluation board PCB, as shown in Figure 46 with V1, V2, V3, V4, and V5. V3 was used as the reference point, and all values are referenced to probe V3.

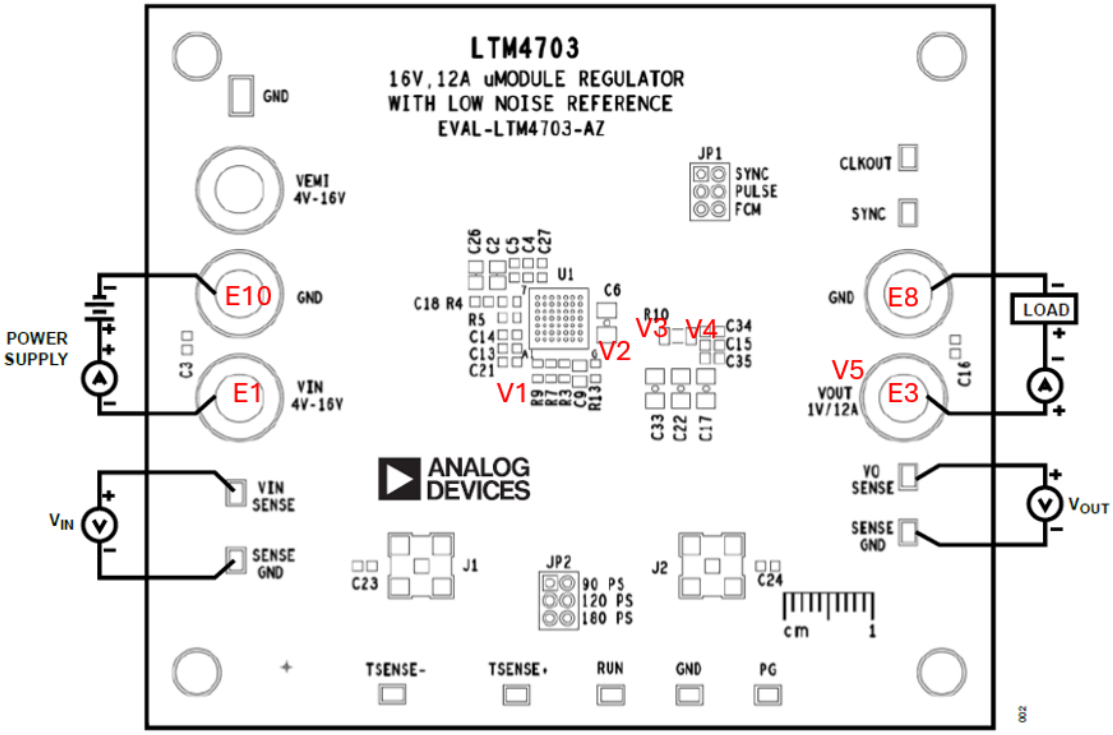


Figure 46 Voltage measurement points and Voltage Probe naming.

V1 (mV)	V2 (mV)	V3 (mV) "REF"	V4 (mV)	V5 (mV)
0.82	0.52	0.00	0.16	1.03
1.61	1.01	0.00	0.38	2.13
2.43	1.52	0.00	0.58	3.22
3.27	2.04	0.00	0.78	4.32
4.12	2.57	0.00	0.99	5.46
4.99	3.11	0.00	1.20	6.60
5.88	3.67	0.00	1.43	7.80
6.80	4.25	0.00	1.65	9.02
7.75	4.83	0.00	1.88	10.27
8.73	5.45	0.00	2.12	11.59
9.73	6.07	0.00	2.36	12.90
10.63	6.63	0.00	2.59	14.10

Table 2 Voltage Measurements

A subsequent measurement was conducted at the output of the resistor. This serves as the primary output Copper Plane for Vout and will be utilized to examine further effects during simulations.

Measurements were conducted on V1, V2, V4, and V5, all relative to V3.

Iout (A)	V4-5 (mV)
1.00	0.87
2.00	1.79
3.00	2.63
4.00	3.53
5.00	4.46
6.00	5.39
7.00	6.37
8.00	7.37
9.00	8.39
10.00	9.45
11.00	10.52
12.00	11.50

Table 3 Voltage Drop after Resistor R10

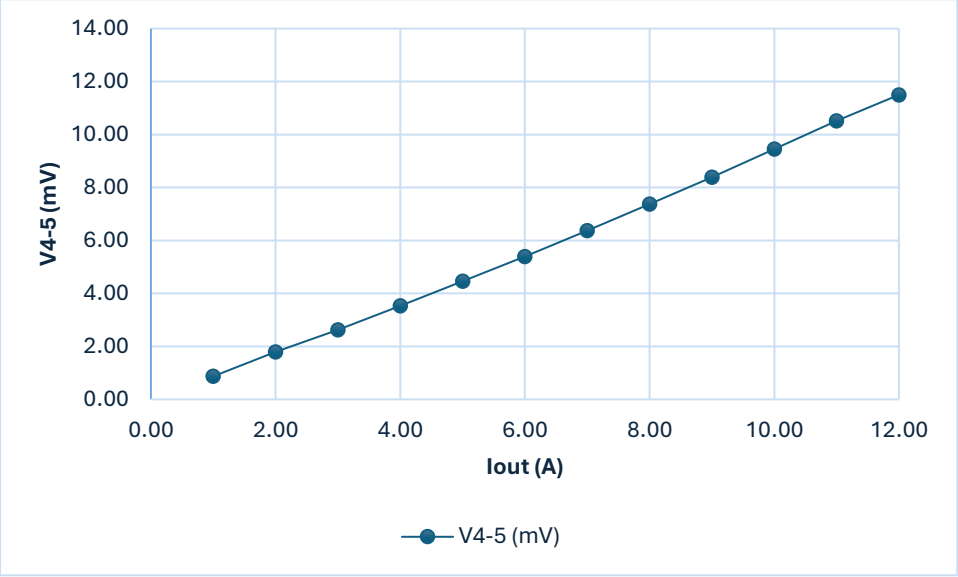


Figure 47 Voltage Drop after Resistor to E3

v. *Temperature measurements*

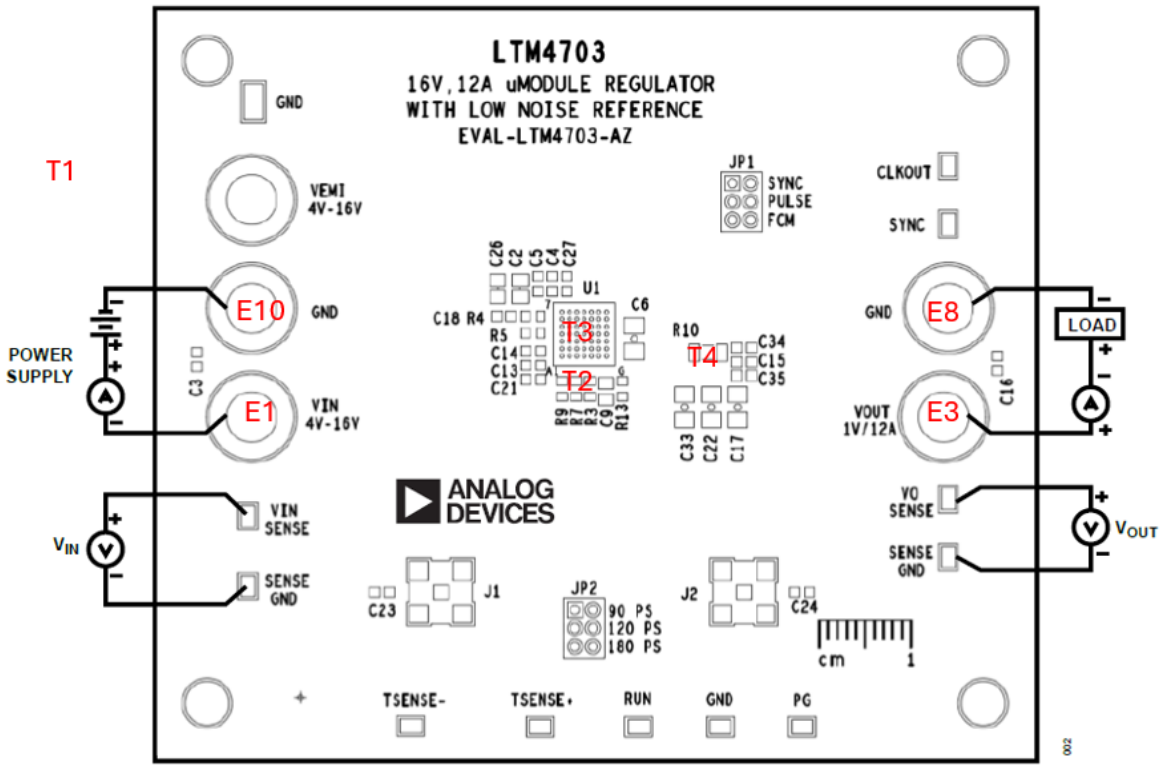


Figure 48 Thermocouple locations

Temperatures were recorded as follows: T1 is the ambient temperature, T2 is beside the DUT, T3 is on top of the DUT, and T4 is on top of Resistor R10.

T1 (ºC)	T2 (ºC)	T3 (ºC)	T4 (ºC)
25.0	35.2	29.7	26.7
25.0	36.1	30.6	27.4
25.0	37.9	32.3	28.8
25.0	39.0	34.1	29.9
25.0	41.1	36.5	31.8
25.0	42.9	39.2	33.2
25.0	45.5	42.5	35.7
25.0	47.7	45.9	37.7
25.0	50.4	49.7	40.0
25.0	55.9	55.1	43.7
25.0	58.2	59.9	46.0
25.0	61.2	64.6	48.5

Table 4 Temperature Measuements

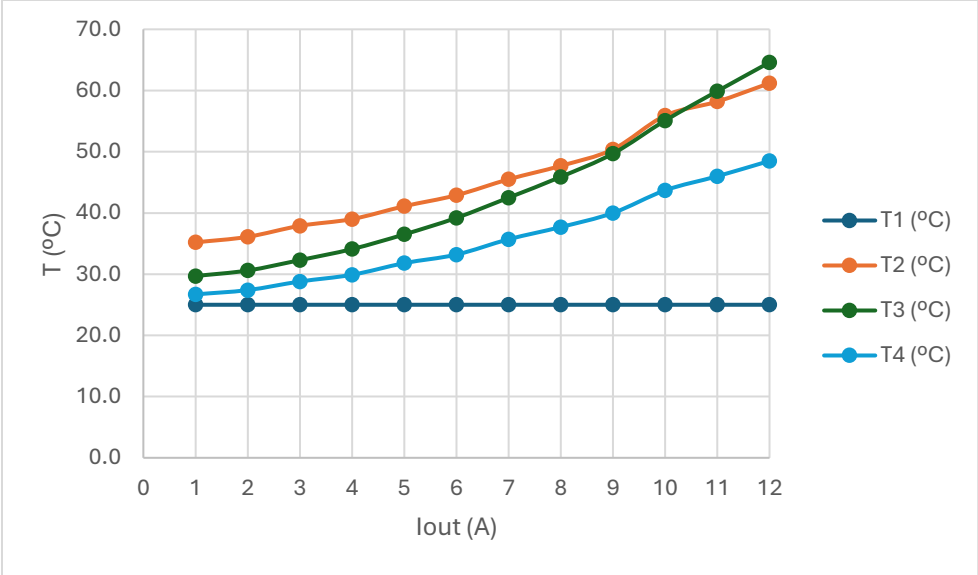


Figure 49 Thermocouple Measurement Plots at Different Current Outputs

D. Calculations from measured data:

i. Circuit Block Diagram

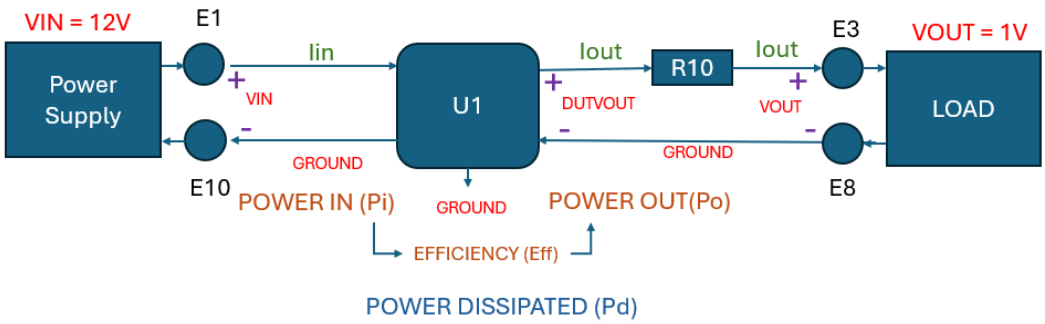


Figure 50 Electrical Definitions and Names

Pin = Vin * Iin

Pout = Vout * Iout

Eff = Po / Pi

Pd = Pi – Po

Using input and output voltages and currents, we can calculate the total power in and out of the board. This allows us to determine DUT's efficiency and estimate its total power loss.

CALCULATIONS FROM MEASUREMENTS			
Pin = Vin * Iin	Pout = Vout * Iout	Eff = Pout / Pin	Ploss = Pin - Pout
Pin (W)	Pout (W)	Eff	Ploss (W)
1.32	1.00	76%	0.32
2.28	2.00	88%	0.28
3.36	3.00	89%	0.36
4.44	4.00	90%	0.44
5.52	5.00	91%	0.52
6.72	6.00	89%	0.72
7.92	7.00	88%	0.92
9.12	8.00	88%	1.12
10.32	9.00	87%	1.32
11.52	10.00	87%	1.52
12.84	11.00	86%	1.84
14.04	12.00	85%	2.04

Table 5 Calculated Values from Measurements

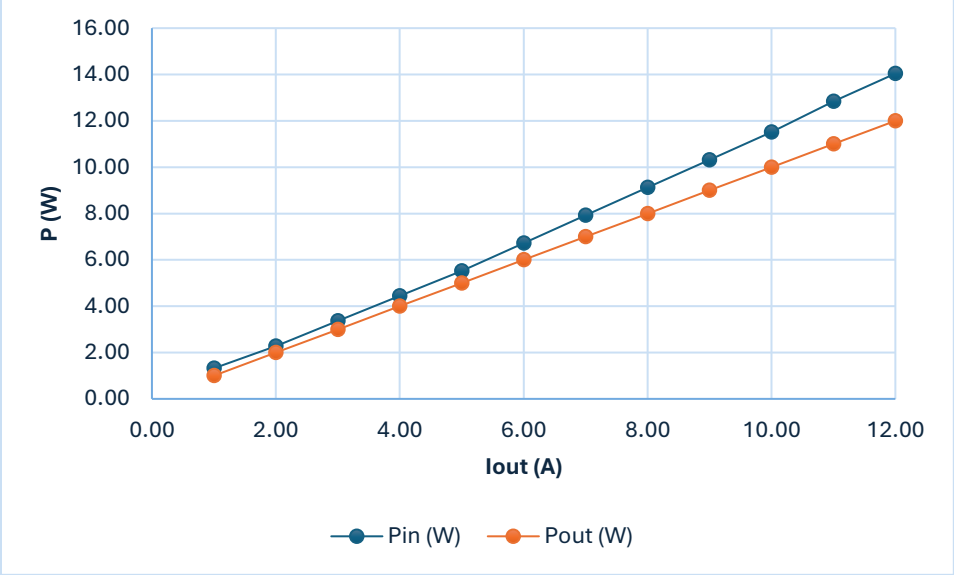


Figure 51 Power Input and Power Output at different Current Outputs

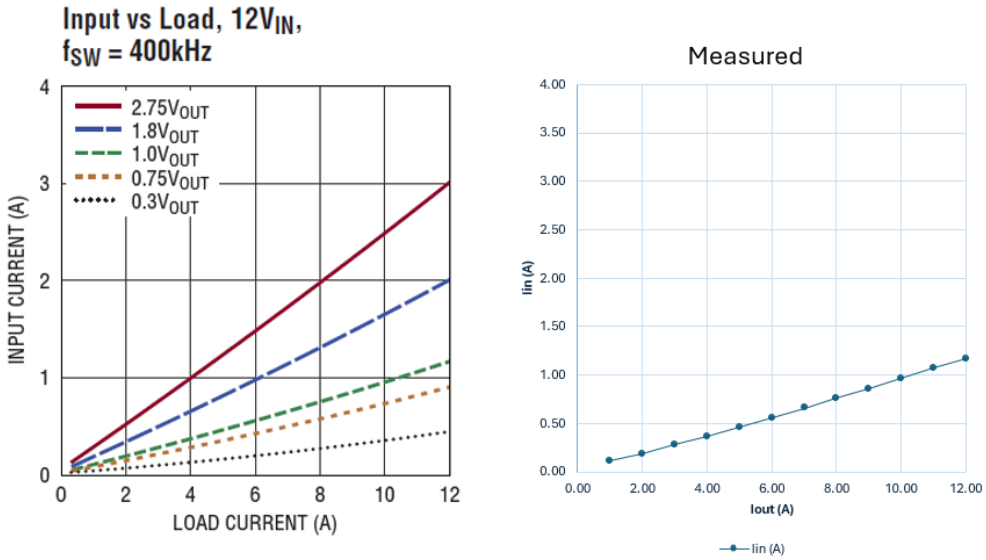


Figure 52 Input Current from Datasheet (left) and Measured Data (right)

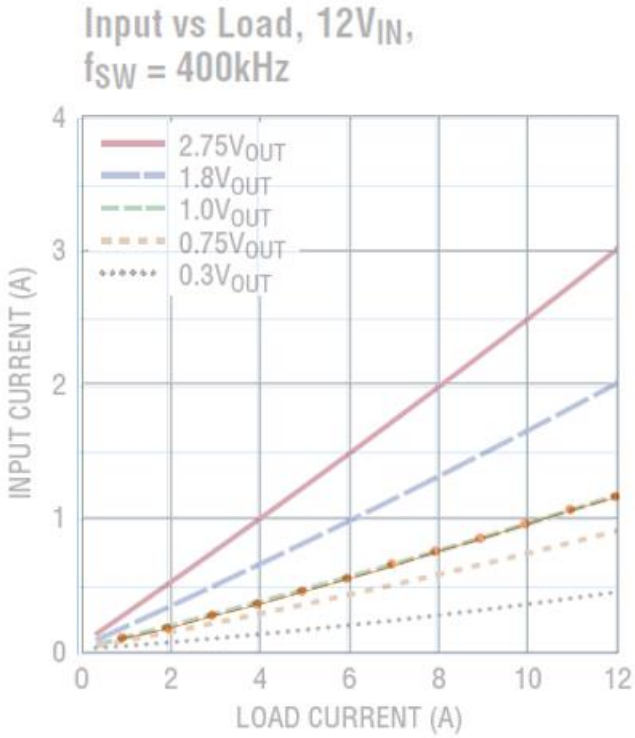


Figure 53 Input Current from datasheet overlapped with Measured Data (orange)

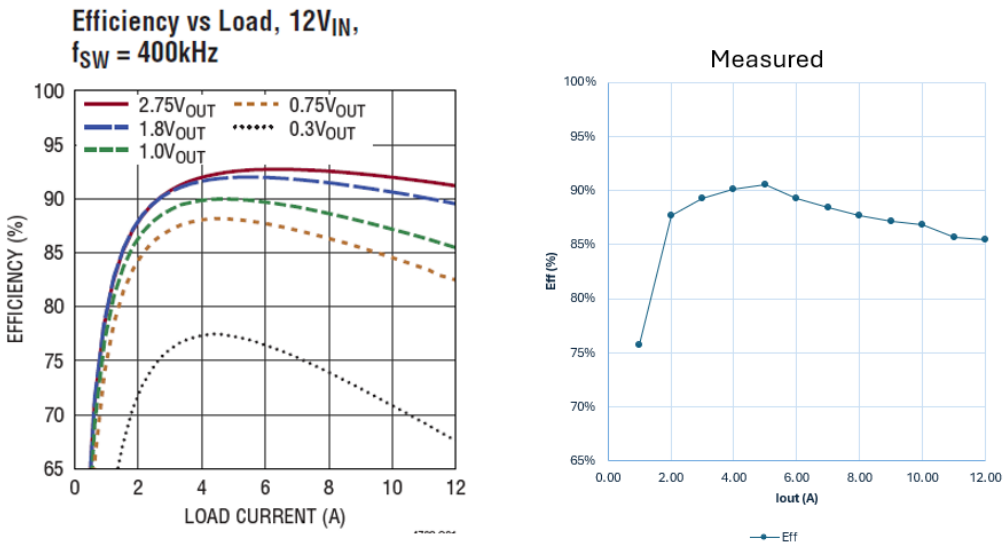


Figure 54 Efficiency from Datasheet (left) and Measured/Calculated Data (right)

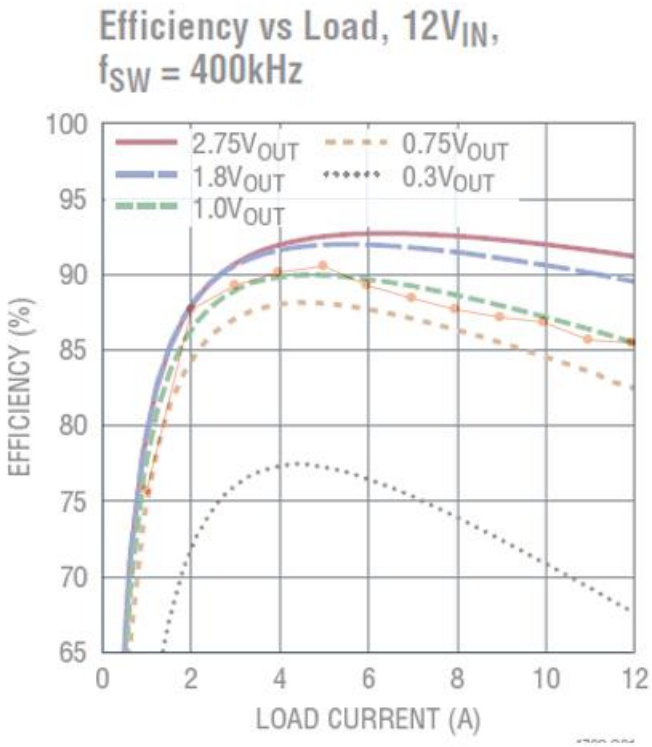


Figure 55 Efficiency from Datasheet Overlapped Measured/Calculated Data (orange).

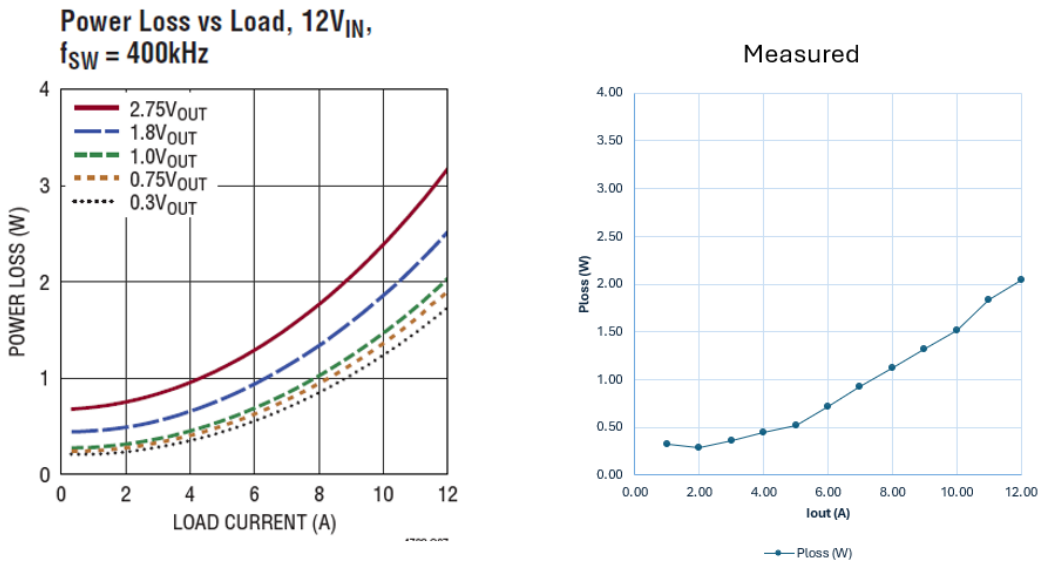


Figure 56 Power Loss from Datasheet (left) and Measured Data (right).

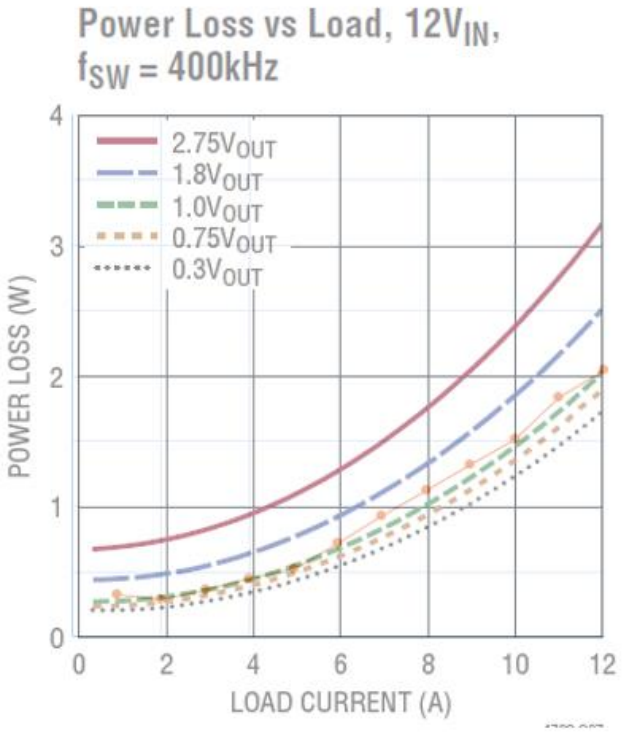


Figure 57 Power loss Overlapped with Measured Data (orange).

V. Simulation

A. Simulation Setup:

Various simulation setups were created to achieve specific current outputs and power dissipation on U1. Currents were based on values from Table 1 and Table 5 using Iin, Iout, and Ploss from the measured data in the tables. This approach ensured controlled records of each setup and individualized plots for further analysis. Figure 58 shows 12 simulation files, named by load currents.

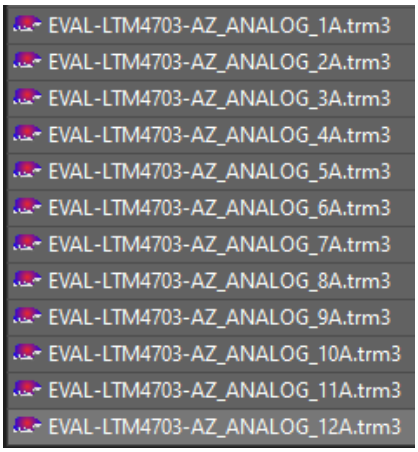


Figure 58 TRM Simulations

An example of the loads table is shown in Figure 59. The node from U1 to R10 is named "DUT_VOUT," and from the resistor R10 to the banana jack E3, it is called "VOUT." This is the loads table on TRM for the 1 Amp output. The power dissipated by U1 is 0.32 Watts, as shown in Table 5. The total amperes for the current input and output can be found in Table 1. In the ampere column, the total sum of amps should always be zero. Conventional current flow indicates that positive values represent where the current is coming out, and negative values indicate the load (sink). In this scenario, the GND net was also considered; typical simulation software does not take the ground into consideration.

Index	Name	PosX (mm)	PosY (mm)	DimX (mm)	DimY (mm)	Height (mm)	Begin	End	Material	Form	K/W-board	K/W-air	Watt	Celsius	Ampere
68	U1	43.611	42.722	6.25	6.25	3.1	0	0	Comp_diel_loc$TRM	r	-1	-1	0.32		
112	DUTVOUT~R10-1	58.698	43.815	0.833	-1	2	1	1	Cu$TRM	c	-1	-1			-1
114	DUTVOUT~U1-A1	44.336	43.447	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			0.125
115	DUTVOUT~U1-A2	44.336	44.247	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			0.125
116	DUTVOUT~U1-A3	44.336	45.047	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			0.125
117	DUTVOUT~U1-B3	45.136	45.047	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			0.125
118	DUTVOUT~U1-F3	48.336	45.047	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			0.125
119	DUTVOUT~U1-G1	49.136	43.447	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			0.125
120	DUTVOUT~U1-G2	49.136	44.247	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			0.125
121	DUTVOUT~U1-G3	49.136	45.047	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			0.125
160	GROUND~E10-1	10.541	48.641	7.315	-1	2	1	1	Cu$TRM	c	-1	-1			0.11
165	GROUND~E8-1	86.36	48.641	7.315	-1	2	1	1	Cu$TRM	c	-1	-1			1
172	GROUND~U1-B4	45.136	45.847	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			-0.06167
173	GROUND~U1-C4	45.936	45.847	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			-0.06167
174	GROUND~U1-C5	45.936	46.647	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			-0.06167
175	GROUND~U1-C6	45.936	47.447	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			-0.06167
176	GROUND~U1-C7	45.936	48.247	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			-0.06167
177	GROUND~U1-D4	46.736	45.847	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			-0.06167
178	GROUND~U1-D5	46.736	46.647	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			-0.06167
179	GROUND~U1-D6	46.736	47.447	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			-0.06167
180	GROUND~U1-D7	46.736	48.247	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			-0.06167
181	GROUND~U1-E4	47.536	45.847	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			-0.06167
182	GROUND~U1-E5	47.536	46.647	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			-0.06167
183	GROUND~U1-E6	47.536	47.447	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			-0.06167
184	GROUND~U1-E7	47.536	48.247	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			-0.06167
185	GROUND~U1-F4	48.336	45.847	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			-0.06167
186	GROUND~U1-F5	48.336	46.647	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			-0.06167
187	GROUND~U1-G4	49.136	45.847	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			-0.06167
188	GROUND~U1-G5	49.136	46.647	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			-0.06167
189	GROUND~U1-G7	49.136	48.247	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			-0.06167
248	VIN~E1-1	10.541	36.83	7.315	-1	2	1	1	Cu$TRM	c	-1	-1			0.11
255	VIN~U1-A5	44.336	46.647	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			-0.01833
256	VIN~U1-A6	44.336	47.447	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			-0.01833
257	VIN~U1-A7	44.336	48.247	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			-0.01833
258	VIN~U1-B5	45.136	46.647	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			-0.01833
259	VIN~U1-B6	45.136	47.447	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			-0.01833
260	VIN~U1-B7	45.136	48.247	0.406	-1	2	1	1	Cu$TRM	c	-1	-1			-0.01833
273	VOUT~E3-1	85.852	36.83	7.315	-1	2	1	1	Cu$TRM	c	-1	-1			-1
279	VOUT~R10-2	61.698	43.815	0.833	-1	2	1	1	Cu$TRM	c	-1	-1			1

Figure 59 TRM Loads Table for 1 Amp Output

To obtain very accurate results, we take great care of the heat transfer coefficient. Normally, for example, if the input values are not very precise, it is sufficient to take a default value. The heat transfer coefficient is a function of temperature, which we want to know. Therefore, the heat transfer coefficient was calculated for each run. First, the loads table was adjusted, and a preliminary run was conducted at an ambient temperature of 25 ºC, with temperature dependence selected and two update loops chosen. After completing the preliminary run, the total electric power and power dissipated by devices were used to recalculate the heat transfer coefficient.

TRM Offers a Report with extensive information for each layer as shown in Figure 60. These reports are crucial for designers to understand the detailed behavior of the PCB under various conditions. By analyzing the simulation results provided in the TRM reports, designers can make informed decisions about optimizing the board layout, improving thermal management, and ensuring electrical performance. The comprehensive data presented in the reports includes temperature distributions, voltage potentials, and power losses, which are essential for diagnosing issues and enhancing the design's reliability and efficiency. This detailed analysis supports the development of more robust and high-performance PCBs, ultimately contributing to the success of future projects.

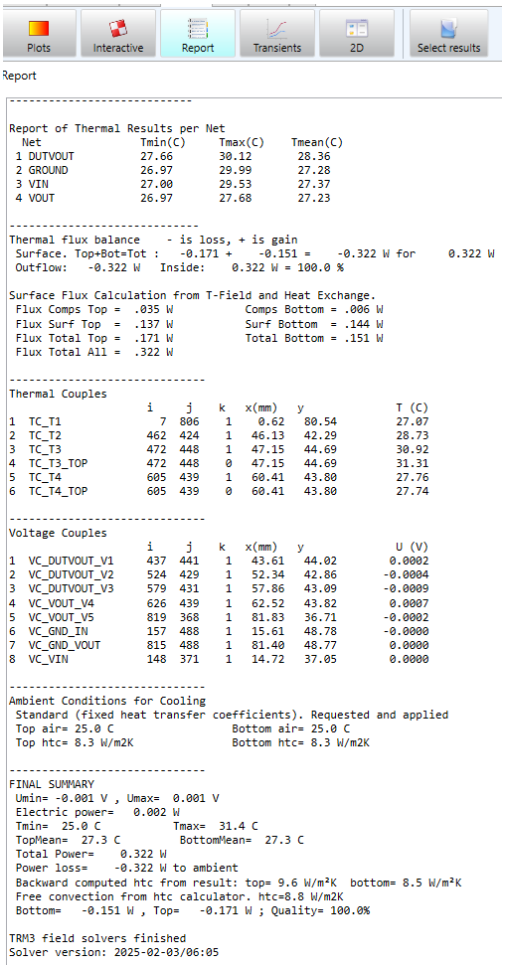


Figure 60 TRM Report

B. Simulation results

The results of the TRM can be visualized through multiple methods and are accessible in a designated folder within the simulation directory. The data is displayed in both tabular format and graphical images, as illustrated in Figure 61.

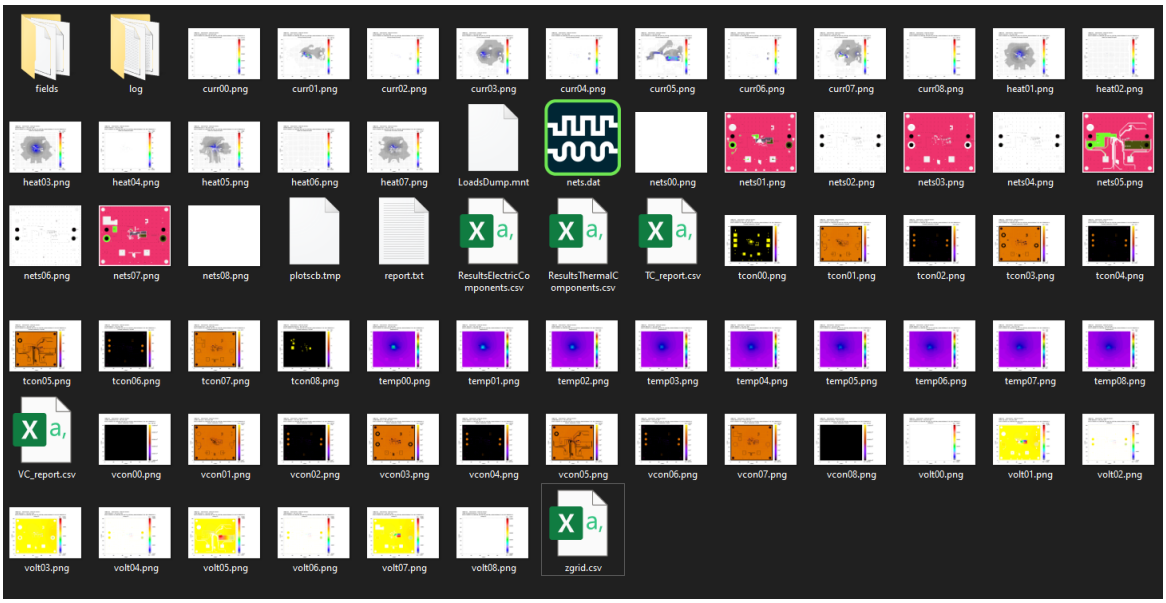


Figure 61 TRM Output Folder

Different layers, shown as Levels in Figure 62, can visualize the information. Variables such as Temperature and Voltage Potentials can be selected in the Variables section.

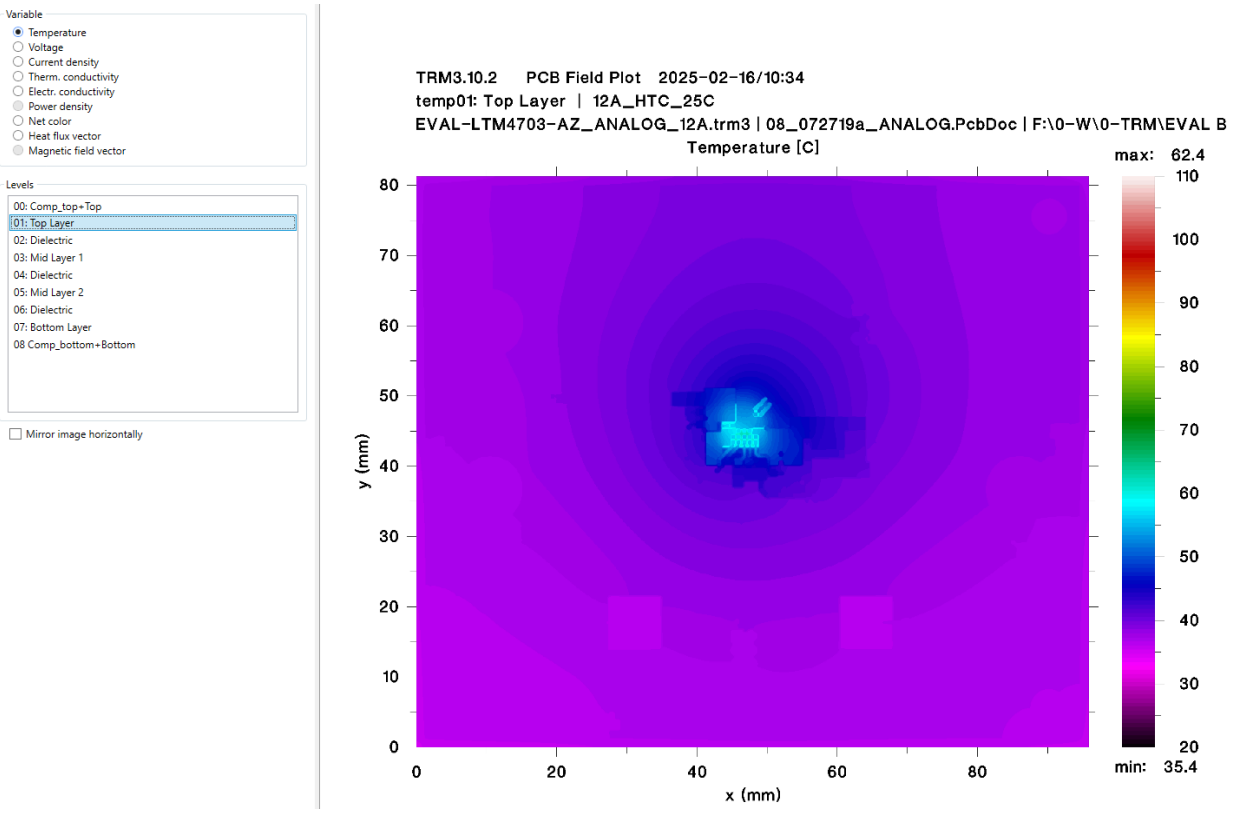


Figure 62 TRM Plots

The Main Menu includes a secondary option labeled "2D". This option offers greater customization, enabling users to modify the Color Palette, adjust the Scale, and overlay the plot with Images.

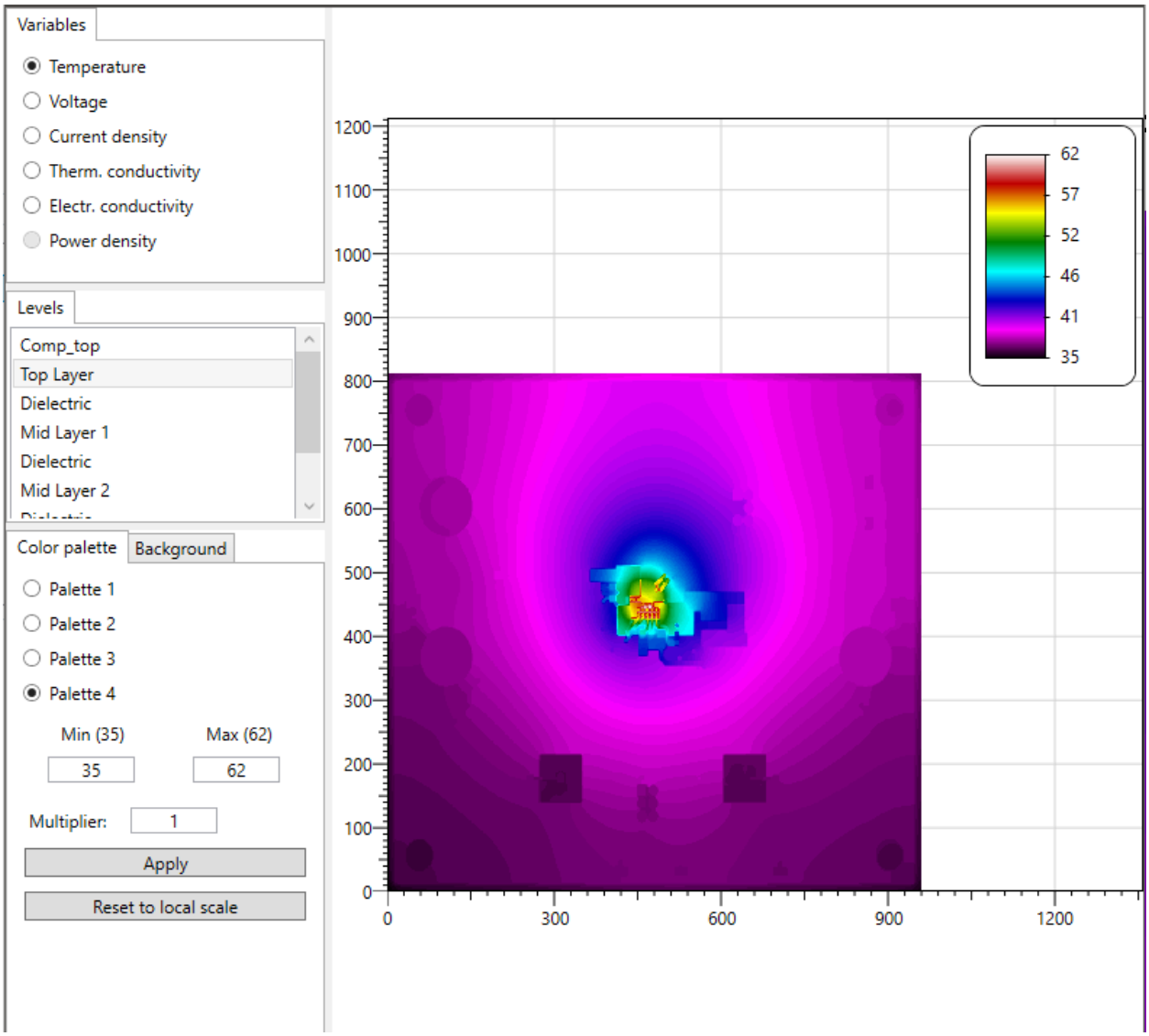


Figure 63 TRM 2D Plots Option

Simulations provide insights that are not visible to the naked eye or measurable without instruments. They allow for internal analysis of each layer of the PCB.

Figure 62 and Figure 63 present how data can be utilized to analyze and comprehend the problem more effectively. This information is typically valuable for designers to understand and adjust PCB (Printed Circuit Board) designs as necessary, and to acquire knowledge for future projects. Although this information is not entirely related to our specific case, the primary objective is to demonstrate that the simulation results can provide significant insights beyond just visual plots of each layer, which are also vital.

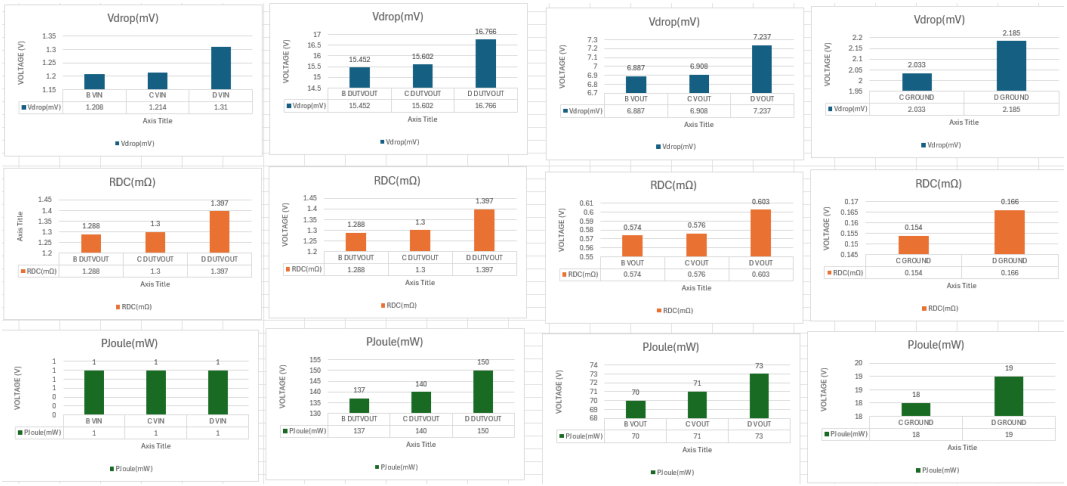


Figure 64 Study and Graphical representation for different Analysis in the Electrical Results (Reference Only)

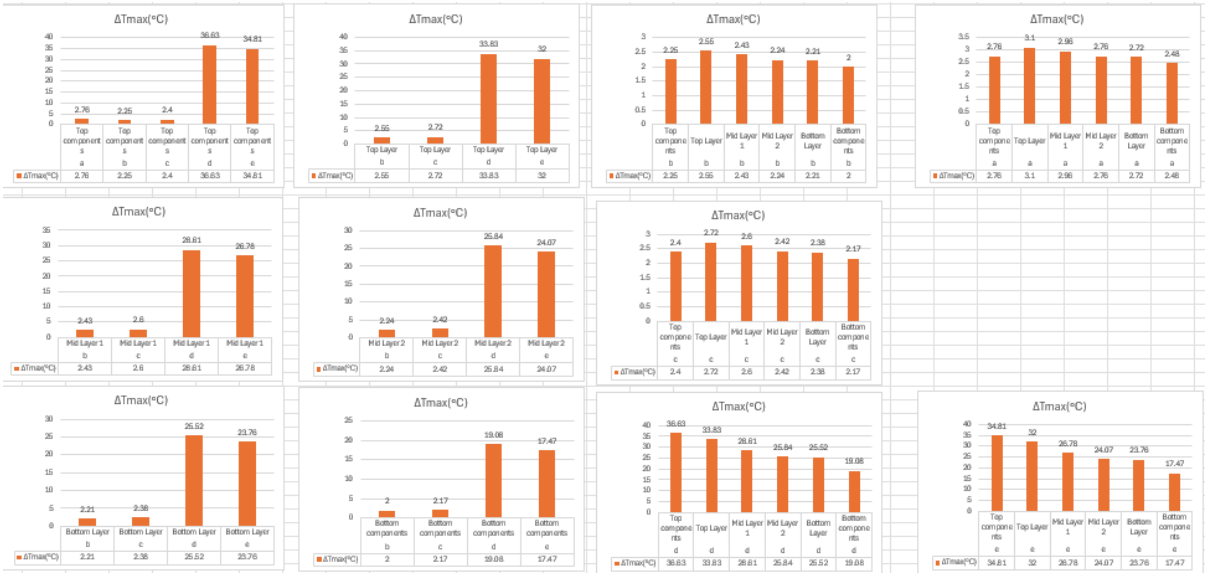


Figure 65 Study and Graphical representation for different Analysis in the Thermal Domain (Reference Only)

C. How to Read and Interpret TRM Results

We will present the information obtained by TRM and highlight several interesting sections. This section covers the las case for the 12Amps output.

The first part of the report provides details about the board and the current simulation setup. The next section shows the simulation results.

The initial part includes voltage potentials. It reports information about each pin or pad in the design, displaying current assignments and voltage potentials.

Additionally, there is a layer-by-layer report in the stackup, as shown in Figure 66, detailing Joule Heating for each layer.

Report by Levels	
0 Top components	0.000 W
1 Top Layer	0.121 W
2 Dielectric	0.007 W
3 Mid Layer 1	0.008 W
4 Dielectric	0.018 W
5 Mid Layer 2	0.093 W
6 Dielectric	0.003 W
7 Bottom Layer	0.034 W
8 Bottom components	0.000 W
Total Joule Heat= 0.285 W	

Figure 66 TRM Report File: Joule Heating by Layer

There is also a summary for each net assigned for simulation as shown in Figure 67.

Report of Electric Results per Net in Traces

	Net	Flux(A)>0	Flux(A)<0	Umin(V)	Umax(V)	Vdrop(mV)	RDC(mOhm)	PJoule(W)	Comment
1	DUTVOUT	12.000	-12.000	-0.006	0.009	14.669	1.222	0.129	
2	GROUND	13.170	-13.170	0.000	9.051	9050.660	687.218	0.022	
3	VIN	1.170	-1.170	-0.001	0.001	1.966	1.680	0.002	
4	VOUT	12.000	-12.000	-0.008	0.004	11.336	0.945	0.132	
	Total Joule Heat							0.285	

Figure 67 TRM Report File: Electric Results per Net

The next section will be for the result of the temperature.

The first section will show the temperature for each component. And like the voltage results TRM will summarize the Temperature by Levels and report the nets included in the simulation.

```
----------------
Report by Levels.                      Tmin(C)    Tmax(C)
  0 Top components                       25.00   65.41
  1 Top Layer                            35.35   62.40
  2 Dielectric                           35.40   58.87
  3 Mid Layer 1                          35.43   57.15
  4 Dielectric                           35.51   55.61
  5 Mid Layer 2                          35.43   54.56
  6 Dielectric                           35.40   54.19
  7 Bottom Layer                         35.35   53.83
  8 Bottom components                    25.00   46.86

----------------------------

Report of Thermal Results per Net
  Net              Tmin(C)     Tmax(C)     Tmean(C)
 1 DUTVOUT         41.99       57.46       46.65
 2 GROUND          36.33       56.36       38.55
 3 VIN             36.44       53.24       38.89
 4 VOUT            36.59       41.88       38.83

----------------------------
```

Figure 68 TRM Report File: Temperature Reports by Levels and Net

If thermocouples and voltage probes are utilized, TRM will also provide a summary.

```
------------------------------
Thermal Couples
                    i     j    k   x(mm)   y             T (C)
1  TC_T1            7   806    1    0.62   80.54         36.80
2  TC_T2          462   424    1   46.13   42.29         48.24
3  TC_T3          472   448    1   47.15   44.69         62.36
4  TC_T4          605   439    1   60.41   43.80         43.01

------------------------------
Voltage Couples
                    i     j    k   x(mm)   y             U (V)
1  VC_DUTVOUT_V1  437   441    1   43.61   44.02         0.0029
2  VC_DUTVOUT_V2  524   429    1   52.34   42.86        -0.0055
3  VC_DUTVOUT_V3  579   431    1   57.86   43.09        -0.0114
4  VC_VOUT_V4     626   439    1   62.52   43.82         0.0092
5  VC_VOUT_V5     819   368    1   81.83   36.71        -0.0022
6  VC_GND_IN      157   488    1   15.61   48.78        -0.0001
7  VC_GND_VOUT    815   488    1   81.40   48.77         0.0005
8  VC_VIN         148   371    1   14.72   37.05         0.0003
```

Figure 69 TRM Report File: Thermocouples and Voltage Probes

The voltage in TRM is presented as the potential difference between two points, with the minus sign indicating the lower potential. Users should calculate the difference between two points, e.g., the voltage difference between VC_VOUT_V4 and VC_VOUT_V5 is 0.0092 - (-0.0022) = 0.0114. It shows that Probe at V4 has higher potential.

D. Simulation Vs Measured

Utilizing the measured data as input for our simulations, we present a comparison of the voltage drops, or voltage potential differences. The node at the Voltage measurement points from V4 and V5 represents the voltage or node after Resistor R10 in the output path. This node was selected because it accurately represents the voltage drop in the PCB for the current output.

Iout (A)	V4-V5 (mV)	TRM V4-V5 (mV)
1	0.87	0.9
2	1.79	1.8
3	2.63	2.7
4	3.53	3.6
5	4.46	4.5
6	5.39	5.5
7	6.37	6.4
8	7.37	7.4
9	8.39	8.3
10	9.45	9.3
11	10.52	10.4
12	11.50	11.4

Table 6 Voltage Comparison (Measured vs Simulated with TRM)

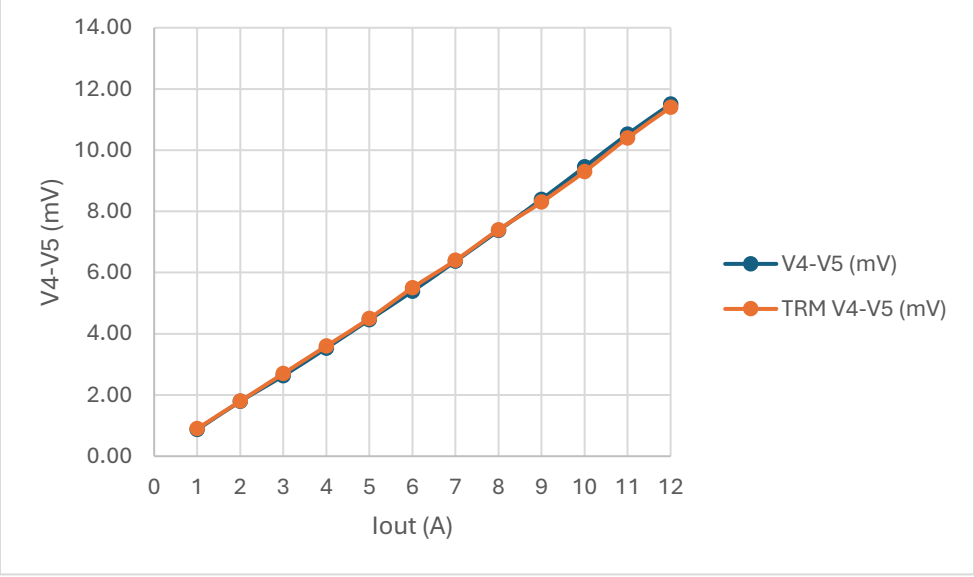


Figure 70 Plots of Voltage Difference from Voltage Measured Point V4 and V5 (Measured vs Simulated by TRM)

Temperature was also compared utilizing the electrical characteristics of the measured data, T3 is the temperature above U1. TRM utilized the average temperature inside the Body.

Iout (A)	T3 (ºC)	TRM T3 (ºC)
1	29.7	30.92
2	30.6	30.26
3	32.3	31.77
4	34.1	33.33
5	36.5	34.87
6	39.2	38.51
7	42.5	42.18
8	45.9	45.83
9	49.7	49.47
10	55.1	53.09
11	59.9	58.78
12	64.6	62.36

Table 7 Temperature Comparison above U1 (Measured vs TRM Simulation)

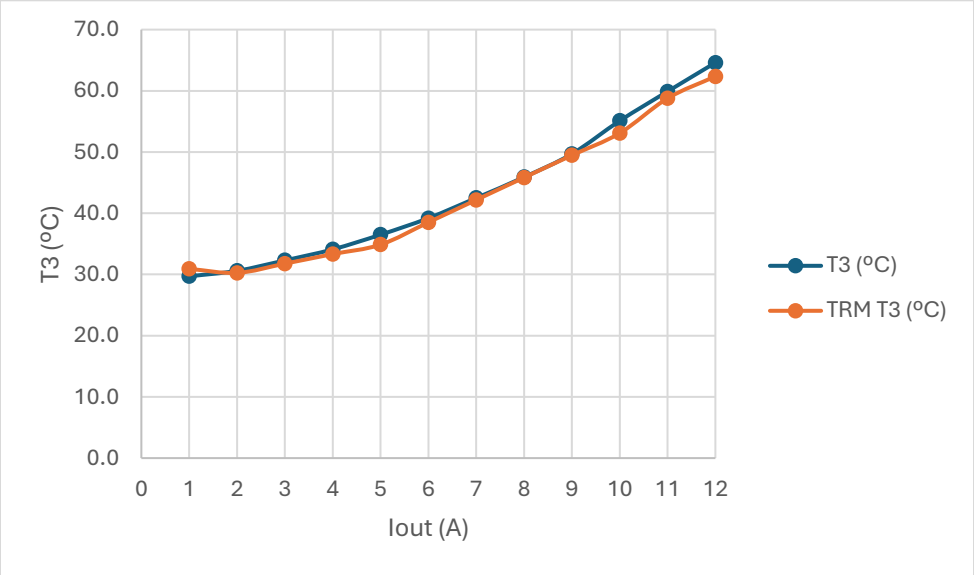


Figure 71 Temperature Plot above U1 (Measured vs TRM Simulation)

Figure 72 Thermal Image at 12Vin, 1V, 12A Output, No Airflow (From Datasheet [3])

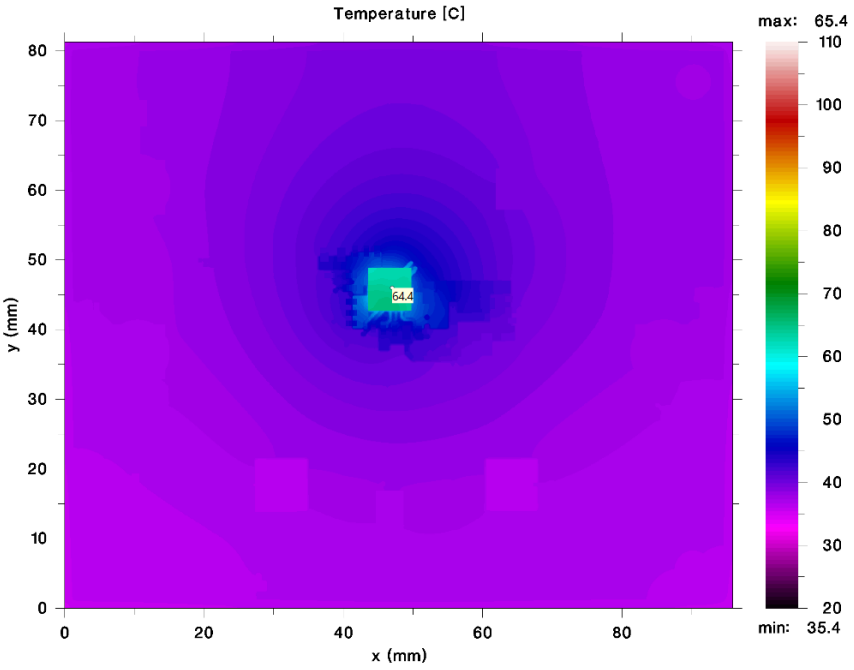


Figure 73 TRM Simulation Temperature plot at 12Vin, 1V, 12A Output, No Airflow

E. Complete Set of thermal Results

The subsequent section will present images depicting the outcomes for various layers and variables within the Results Tab of TRM. These can be considered as elements that are imperceptible to the naked eye or unmeasurable by instruments. These components, referred to as the hidden parts within our electronic devices, are observable exclusively through simulation.

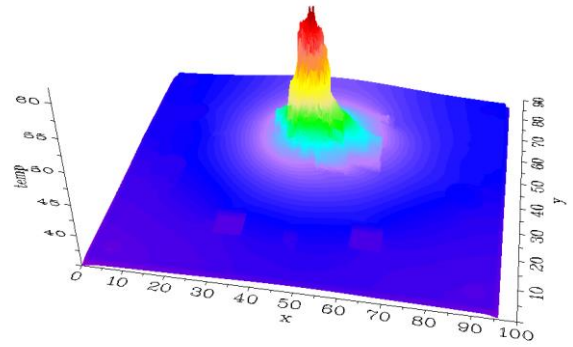
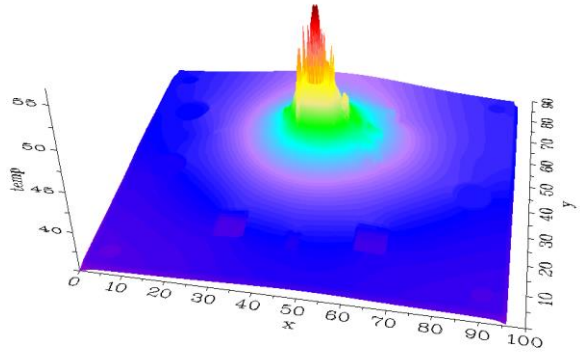
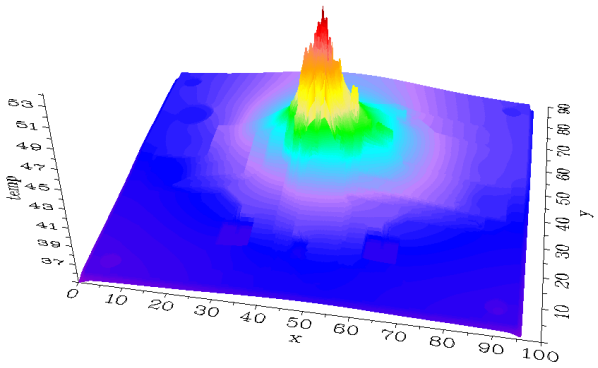
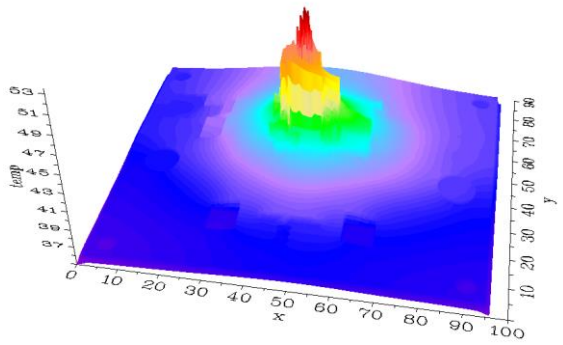
Temperature in °C (3D View)	Layer
	Top Layer
	Layer 2
	Layer 3
	Layer 4

Figure 74 TRM Results: 3D Temperature Plots for All Layers

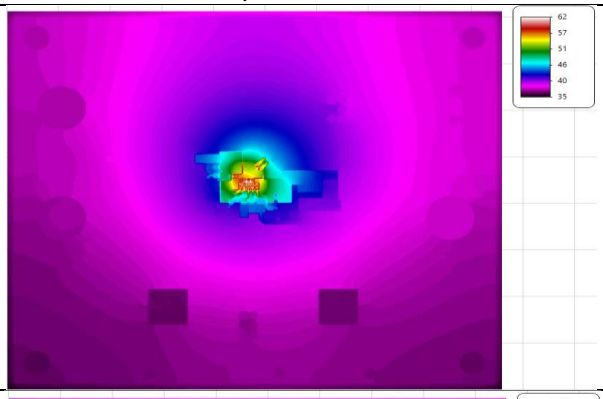
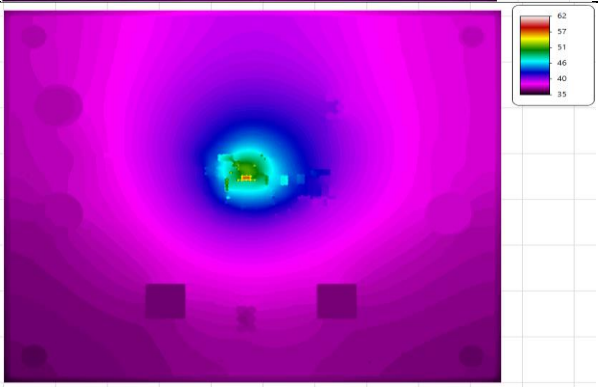
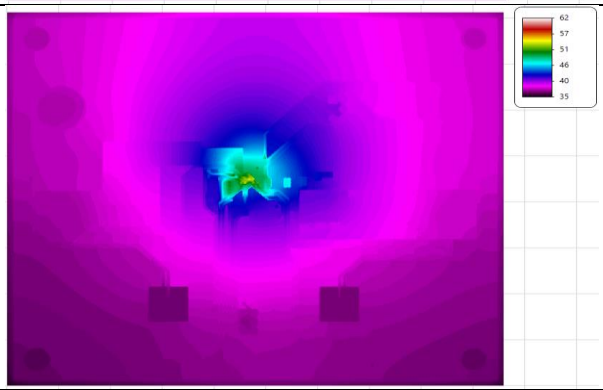
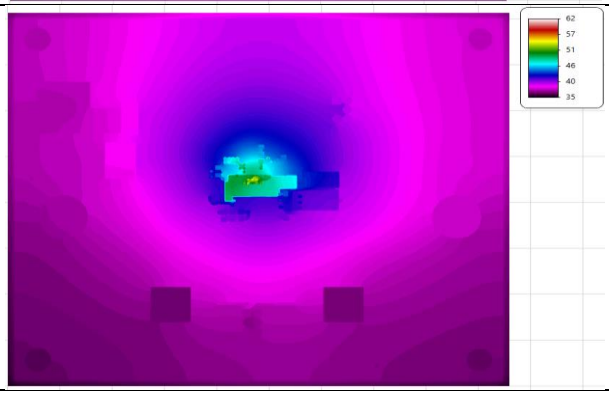
Temperature in °C	Layer
	Top Layer
	Layer 2
	Layer 3
	Layer 4

Figure 75 TRM Results: 2D Temperature Plots for All Layers

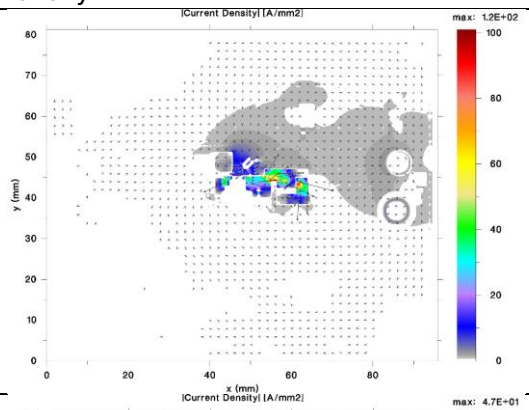
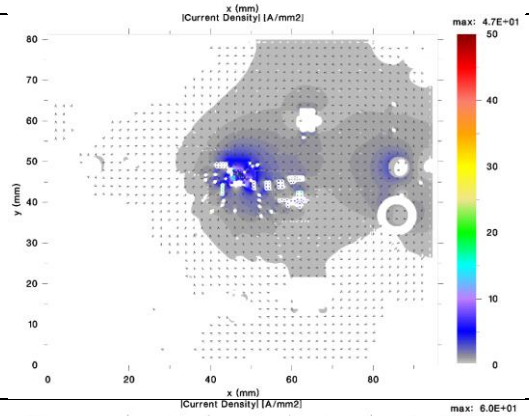
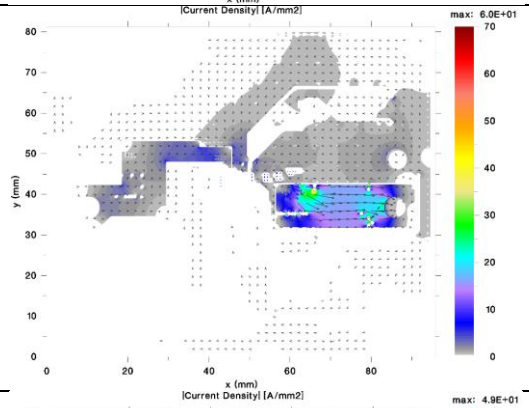
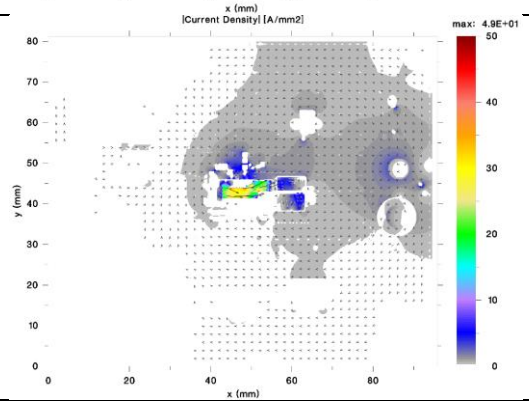
Current Density in A/m^2	Layer
	Top Layer
	Layer 2
	Layer 3
	Layer 4

Figure 76 TRM Results: Current Density Plots for All Layers

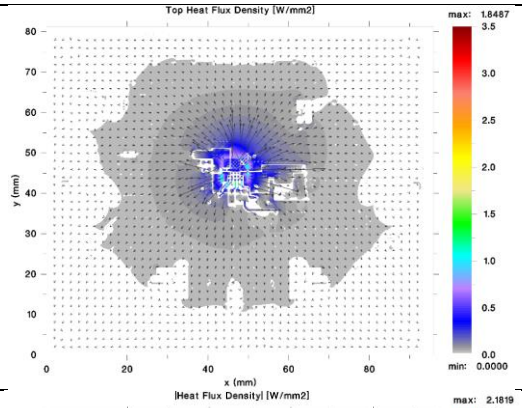
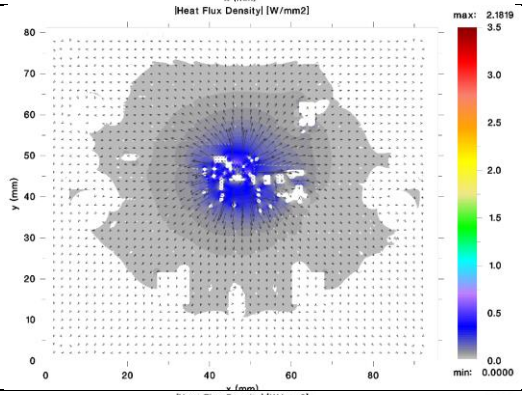
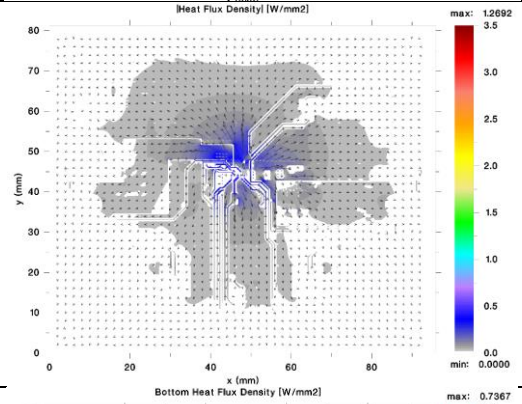
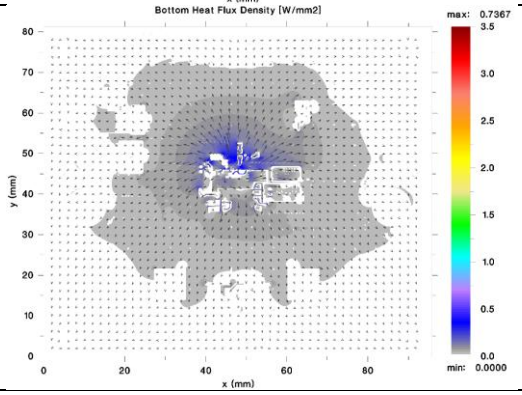
Heat Flux in W/m^2	Layer
	Top Layer
	Layer 2
	Layer 3
	Layer 4

Figure 77 TRM Results: Heat Flux Plots for All Layers

F. How the PCB heats up

It is crucial to comprehend how your PCB board will perform under specific conditions. One essential parameter is understanding the rate at which your board heats up or, in other words, determining the time required for your board to reach its maximum temperature without altering the conditions.

The thermal time constant of thermal systems quantifies the speed at which a system heats up or cools down. Like the electrical time constant for capacitors and resistors, it is affected by factors such as material density, specific heat capacity (hardly to find for FR4 and Components in a datasheet), volume, exposed surface area, and total heat transfer coefficient. Essentially, it indicates the time necessary for a system to achieve approximately 63.2% of its total temperature change when subjected to heating or cooling. This concept is vital for analyzing and optimizing thermal behavior in systems such as PCBs.

How quickly the individual regions of the PCB heat up also depends on how the heat can spread locally and how heat spreading is influenced by the other components. This can only be predicted by computer simulation.

Figure 78 shows that it requires approximately 10 minutes for the board to stabilize or reach equilibrium. This information is useful for making accurate measurements, predicting behavior, and understanding how the board will perform in the field.

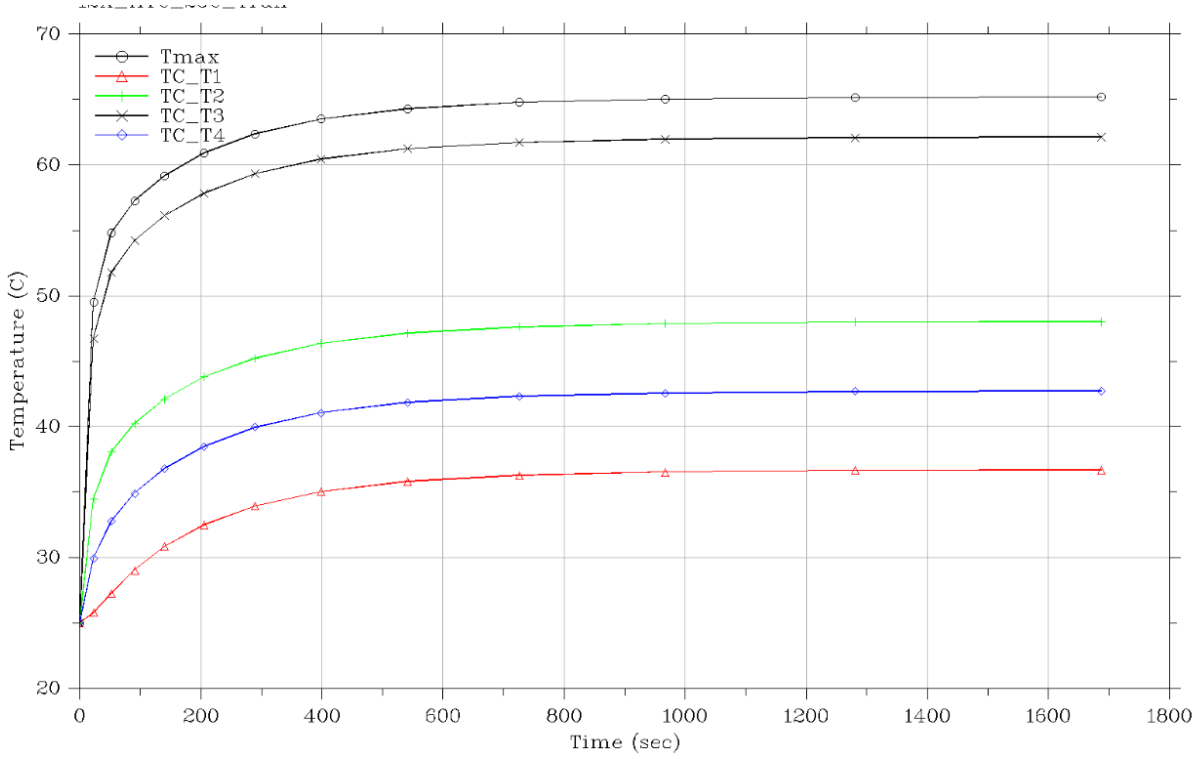


Figure 78 TRM Transient Simulation

G. Excursion

The subsequent section focuses on a topic of particular interest to the authors. We aim to determine if it is possible to predict the behavior of this specific board size and make rough estimates without having the actual PCB traces, planes, and vias in the design.

Component wattage significantly affects current flow in PCB traces and planes, resulting in some heat dissipation. The ground net can also help distribute heat more evenly.

The following letters will represent different conditions in the next figure. Various setups have been created, and the temperature on device U1 has been calculated. The figure illustrates the combinations of these variations. The number 0 indicates that an option is not added or enabled in a particular simulation, while the number 1 shows that an option or feature is active.

Variable and Condition Nomenclature:

W<0/1>: Watts in Component. Represents the watts assigned to U1 in the design.

T<0/1>:: Main Current in Traces. Indicates if currents are assigned to the nets, input, and output paths.

G<0/1>:: Current in Ground Net. Indicates if currents are assigned to the ground net.

PLANE<0/1>:: Solid Plane in Simulation. A special condition where a solid plane is drawn in different board layers to show maximum copper coverage for that layer.

Consider the initial plot condition, W0,T0,G1. This indicates that no watts are assigned to the component, there is no current in any of the active traces, but current has been added to the ground connection. Although this does not represent actual real-world conditions, it will help us understand different scenarios.

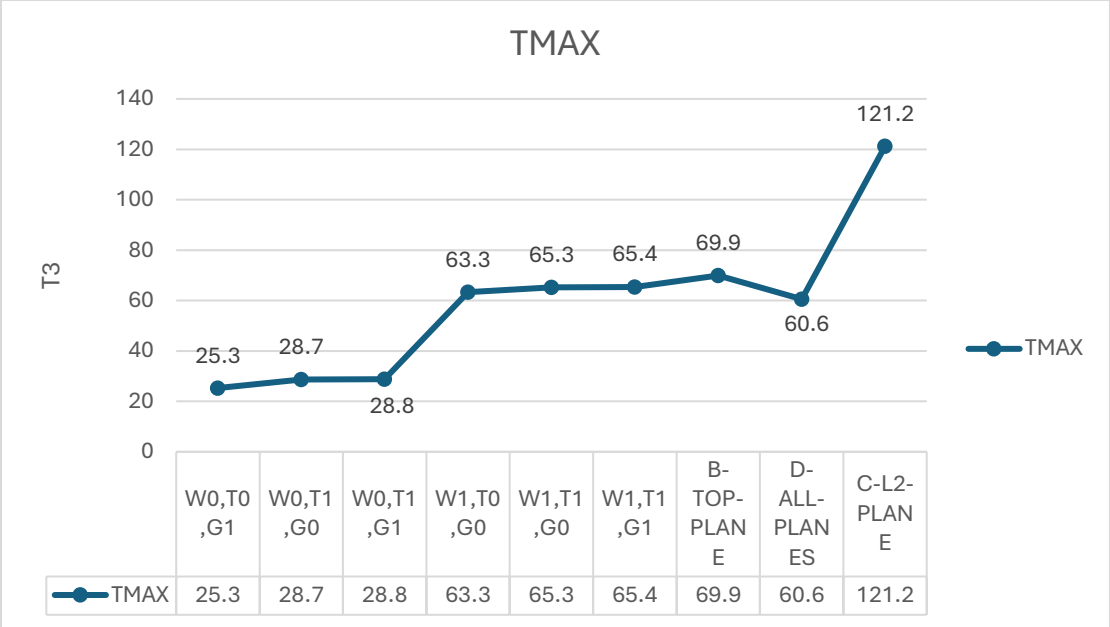


Figure 79 Simulation Experiment for PCB estimations

Based on measurements, simulations, and PCB inspections, the maximum temperature is approximately 64 degrees. The graph shows this condition occurs when the components have assigned watts and the nets have assigned currents. Adding a solid plane to the top layer results in a difference of about 5 degrees. The solid plane represents the maximum copper condition or maximum power dissipation through the board. Adding solid planes to all layers also yields a difference of 5 degrees Celsius.

H. Temperature Increase by the watt ratio

The increase in temperature of the device relative to the total power dissipated provides an ideal condition for predicting the temperature rise due to a given power dissipation. This is accurate only for this specific board based on actual measurements.

Table 8 illustrates the temperature difference relative to ambient temperature in column 3. Column 5 presents the ratio of this temperature difference at each current output concerning the power dissipated by the device. This concept is analogous to the thermal resistance of the device to the ambient (θJA); however, in this instance, it reflects the actual thermal resistance of the device to both the ambient and the board. This may also be referred to as the thermal impedance of the device, though it is primarily valid under these specific conditions and board design.

Iout (A)	T3 (ºC)	DeltaT3 (ºC)	Ploss (W)	DT3/Ploss (ºC/W)
1	29.7	4.7	0.32	14.7
2	30.6	5.6	0.28	20.0
3	32.3	7.3	0.36	20.3
4	34.1	9.1	0.44	20.7
5	36.5	11.5	0.52	22.1
6	39.2	14.2	0.72	19.7
7	42.5	17.5	0.92	19.0
8	45.9	20.9	1.12	18.7
9	49.7	24.7	1.32	18.7
10	55.1	30.1	1.52	19.8
11	59.9	34.9	1.84	19.0
12	64.6	39.6	2.04	19.4

Table 8 Temperature increases by a given power

Datasheet [4] shows a θJA = 19.6 °C/W, the average of Column 5 on Table 8 shows a value of 19.3 °C/W which is close to what is shown in datasheet.

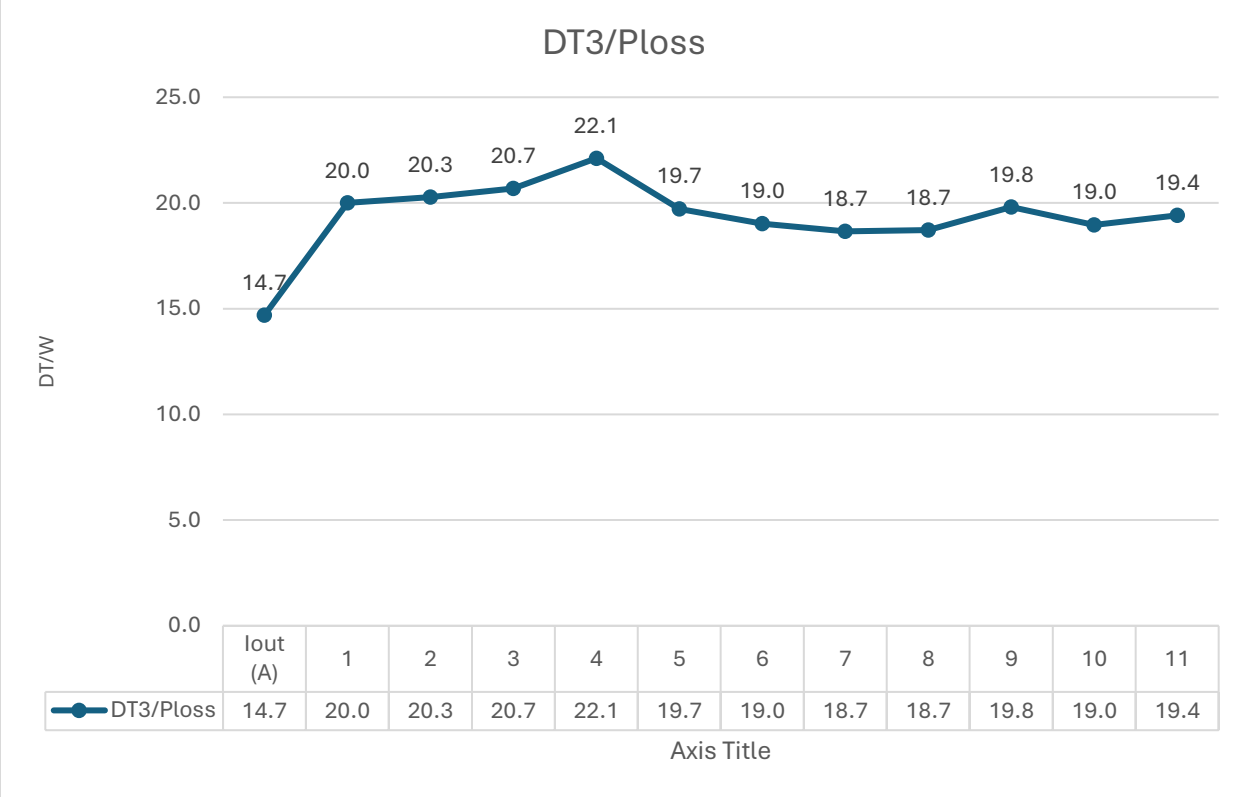


Figure 80 Temperature Increase Ratio to Watts

Conclusions

The study on the EVAL-LTM4703-AZ evaluation board highlights the critical importance of thermal management in high-current switching regulators. The compact design and high-power density of the LTM®4703 µModule® regulator make it an ideal candidate for analyzing thermal challenges. Through theoretical modeling, experimental validation, and simulation, the study comprehensively assesses temperature rise and associated phenomena.

Key findings include:

1. **Power Loss and Efficiency**: The efficiency of the LTM®4703 µModule® regulator is approximately 86% under specified operating conditions, with power loss primarily attributed to conduction losses in the power MOSFETs, switching losses, and core losses in the integrated inductor.
2. **Thermal Profiles**: Temperature measurements indicate a significant temperature rise under operational stress, with the device's performance decreasing at higher temperatures. The thermal resistance (θJA) of the package is minimized using advanced materials and design techniques, enabling the LTM®4703 to deliver full-rated current without thermal derating.
3. **Simulation Results**: TRM simulations provide insights into the temperature distribution, current density, and heat flux within the PCB. The simulations show that the board requires approximately 10 minutes to stabilize or reach equilibrium. The comparison between measured and simulated data demonstrates the accuracy of TRM in predicting thermal behavior.

Conducting your own experiments and measuring the actual evaluation board is essential for validating simulations. This hands-on method allows engineers to refine their designs based on personal experience and observations. Utilizing TRM (Thermal Risk Management) is particularly advantageous as it provides a comprehensive package that includes PDN IR drop, current density, and thermal analysis. This integrated approach assists engineers in understanding both thermal and electrical effects concurrently, offering a holistic view of the PCB's performance.

Furthermore, TRM enables engineers to observe the internal planes, which is nearly impossible to measure or visualize with current tools such as instruments, infrared cameras, or thermocouples. This capability is invaluable for gaining deeper insights into the internal behaviors of the PCB and making well-informed design decisions.

These findings are intended to assist engineers in optimizing thermal design in high-current switching regulators, balancing power density with thermal reliability. The study highlights the importance of considering both electrical and thermal interactions in PCB design to ensure robust performance.

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