"Proximity Over Quantity: How Copper Plane Placement Outperforms Thermal Via Count in QFN Package Thermal Management"

Abstract

This study fundamentally challenges conventional thermal design orthodoxy by demonstrating that copper plane proximity dramatically outperforms thermal via quantity in QFN package thermal management. Through systematic thermal simulation analysis of 5×5 mm QFN packages across 25 PCB design configurations, we reveal counter-intuitive findings that contradict established industry practices: a single copper plane at 12-mil separation achieves 27°C temperature reduction compared to only 11°C from nine thermal vias, while copper plane placement alone provides 39% temperature improvement versus 23% from maximum via implementation. Our quantitative analysis demonstrates that scaling via size from 6 to 8 mils yields merely 2.5% thermal improvement, while strategic copper plane proximity delivers up to 5× greater thermal benefits. Most significantly, we demonstrate that the presence of a copper plane without thermal vias (43.5°C) results in lower component temperatures than using nine thermal vias without plane proximity (48.2°C). Fundamentally challenging the "More vias means better thermal performance" assumption prevalent in current PCB thermal design guidelines. These findings provide critical design hierarchy guidance: prioritize copper plane proximity over via density, optimize for 4-6 thermal vias rather than extensive arrays, and recognize that multilayer PCB investment yields superior thermal performance compared to 2-layer boards with extensive via implementations. The research delivers immediate industry impact by quantifying thermal design trade-offs that can prevent costly PCB respins and accelerate thermal-critical product development.

1. Introduction

Effective thermal management is essential for reliable electronic systems, especially as devices become smaller and more power-dense. Heat dissipation is particularly challenging in surface-mount packages, where traditional heat sinks are not feasible. QFN packages, common in signal processing and data communication, address these challenges with their compact size and strong electrical performance.

The QFN package architecture features a central thermal pad designed to provide a primary heat conduction path from the die to the PCB, as specified in JEDEC standards for thermal characterization. However, the effectiveness of this thermal path depends heavily on PCB design parameters including copper plane configuration, via implementation, and multilayer stack-up design. While industry's best practices established by IPC standards provide general guidelines [1], the quantitative impact of specific design choices on thermal performance remains poorly understood, with limited systematic studies comparing different thermal management approaches.

This study addresses this knowledge gap through systematic thermal simulation analysis of QFN packages under various PCB design scenarios. Our objective is to provide quantitative data that enables informed thermal design decisions and challenges commonly held assumptions about thermal via effectiveness.

1.1 Related Work

Systematic comparison of copper plane proximity effects versus via-based thermal management remains limited in published literature.

JEDEC JESD51-2A thermal test standards provide standardized methodologies for thermal characterization but focus primarily on package-level metrics rather than PCB design optimization. Our study extends this work by providing comprehensive PCB design guidelines based on systematic thermal simulation analysis.

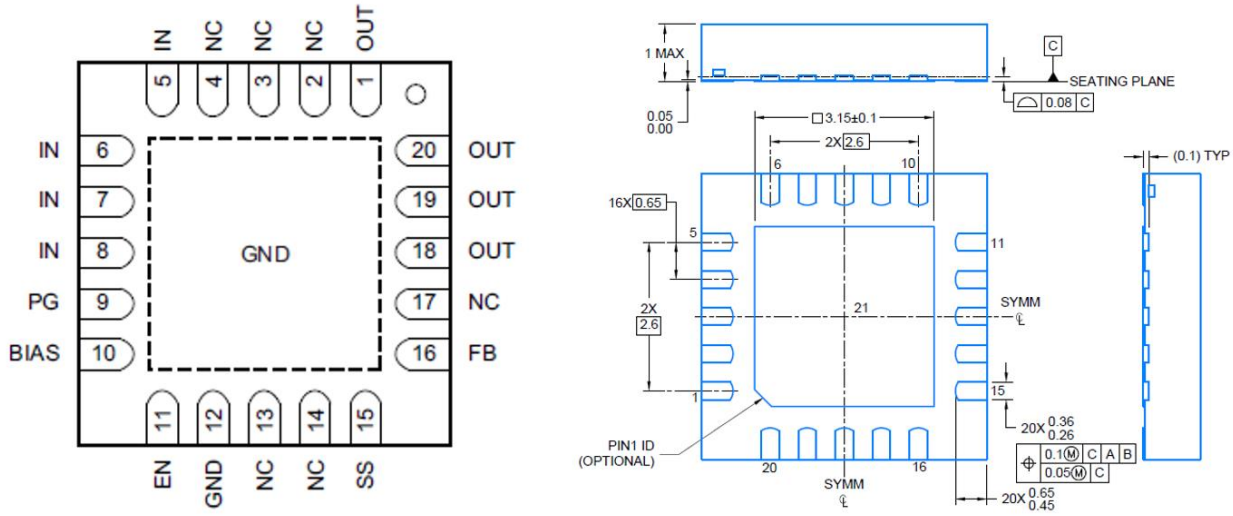


Figure 1 Cross-sectional diagram of 5×5 mm QFN package, showing central thermal pad

1.2 Test Vehicle Selection

We selected a 5×5 mm QFN package with thermal pad as our primary test vehicle, consistent with JEDEC JESD51-5 thermal test board standards. This package size represents a common form factor in modern electronic designs and provides sufficient thermal pad area for meaningful via implementation studies. The package's widespread adoption in low-power applications makes our findings broadly applicable to current design challenges [2].

2. Methodology

2.1 Simulation Platform and Validation

All thermal simulations were conducted using TRM from Adam Research [5].

Mesh Parameters:

- Element size: 0.05mm

Boundary Conditions:

- Natural air-cooling coefficient: 8 W/m^2K (still air, Horizontal orientation)
- Ambient temperature: 25°C

2.2 PCB Test Platform

Our analysis utilizes a standardized PCB test platform.

- **Board dimensions:** 5 inches × 5 inches (127 × 127 mm)
- **Layer count:** 2-layer baseline (with 4-layer variations)
- **Board thickness:** 62 mils (1.57 mm)
- **Copper weight:** 1 oz (35 µm) on all layers
- **Dielectric material:** FR4 (thermal conductivity: 0.3 W/mK)
- **Prepreg thickness:** 12 mils (0.3 mm) for 4-layer configurations
- **Ambient temperature:** 25°C
- **Device power consumption:** 0.3W (representative of typical low-power applications [4])

The large board size minimizes edge effects on thermal spreading, ensuring that our results reflect the thermal performance of the package and immediate PCB area rather than overall board thermal capacity, consistent with JEDEC thermal test methodologies.

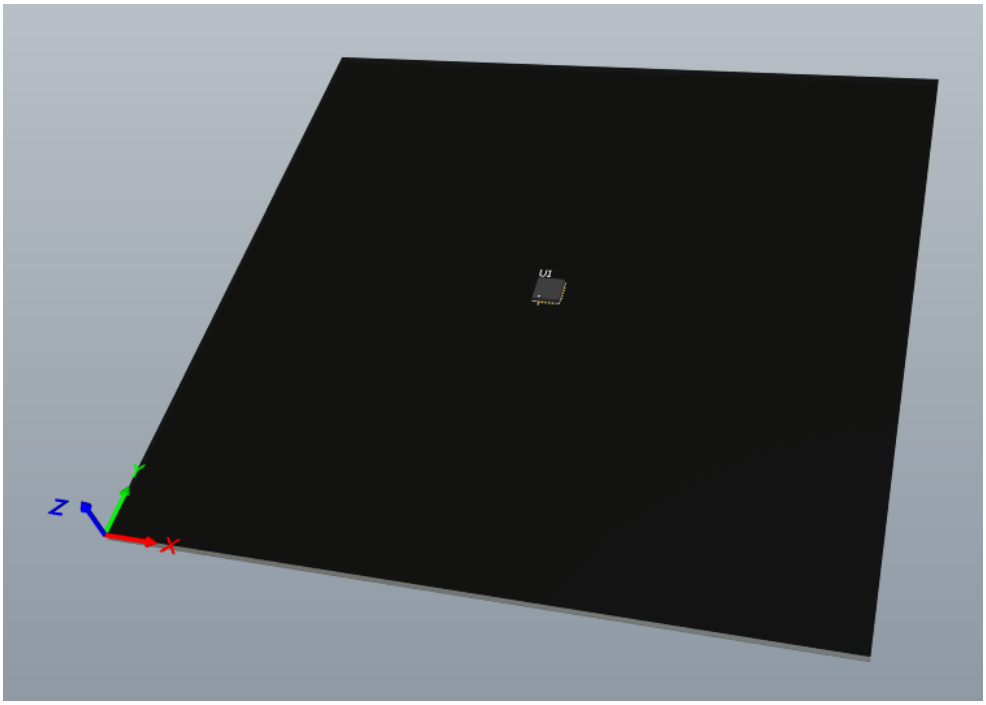


Figure 2 Thermal test board setup showing 127×127 mm PCB with QFN package placement and 62-mil board thickness.

2.3 Design Variations and Nomenclature

We developed a systematic nomenclature to clearly identify test configurations.

Format: x-TOP-y,Bot-z-VIA-s_nVIA

Where:

- **x** = PCB design variation number
- **y** = Top layer copper plane presence (0=absent, 1=present)
- **z** = Bottom layer copper plane presence (0=absent, 1=present)
- **s** = Via diameter (6 or 8 mils)
- **n** = Number of vias

Example: 5-Top-1,Bot-1-VIA-8_9VIA represents PCB design variation 5 with top and bottom copper planes, using 8-mil vias with 9 total vias.

3. Results and Analysis

3.1 Baseline Testing: Impact of Copper Planes (Test 1)

Our initial investigation examined the fundamental impact of copper plane presence on thermal performance. Four basic configurations were tested.

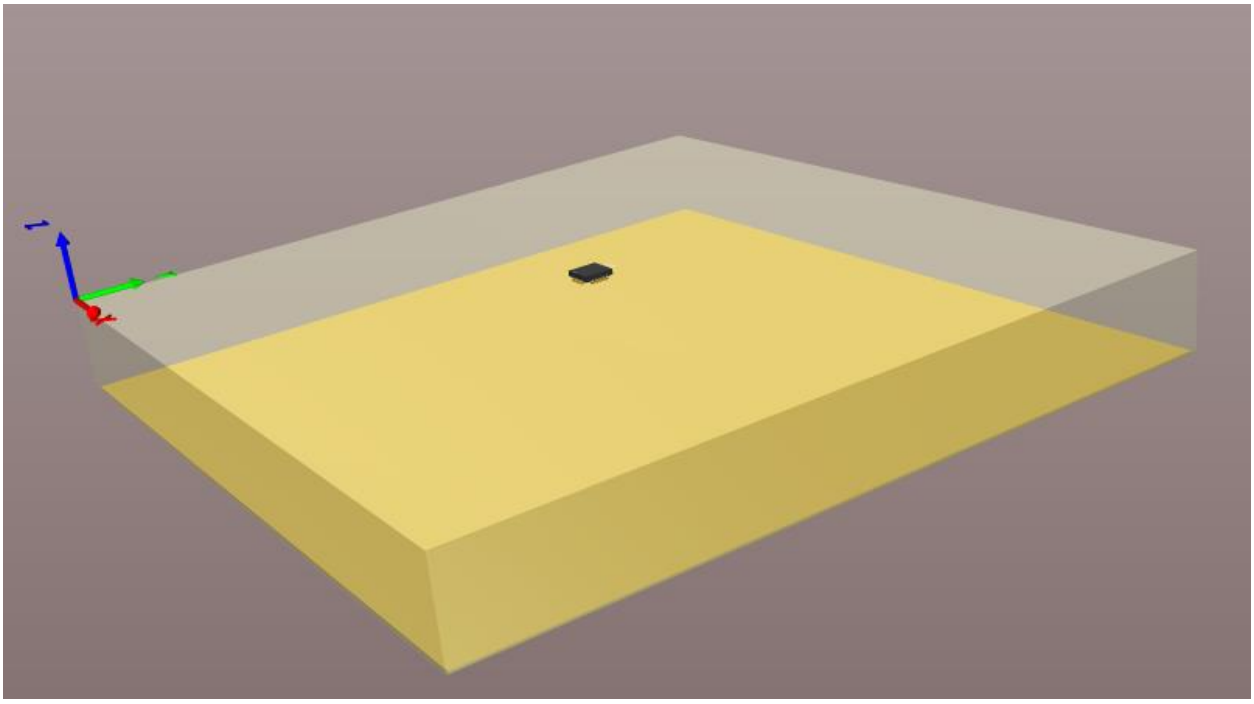


Figure 3 3D Model distribution from baseline thermal simulation of QFN package on test board

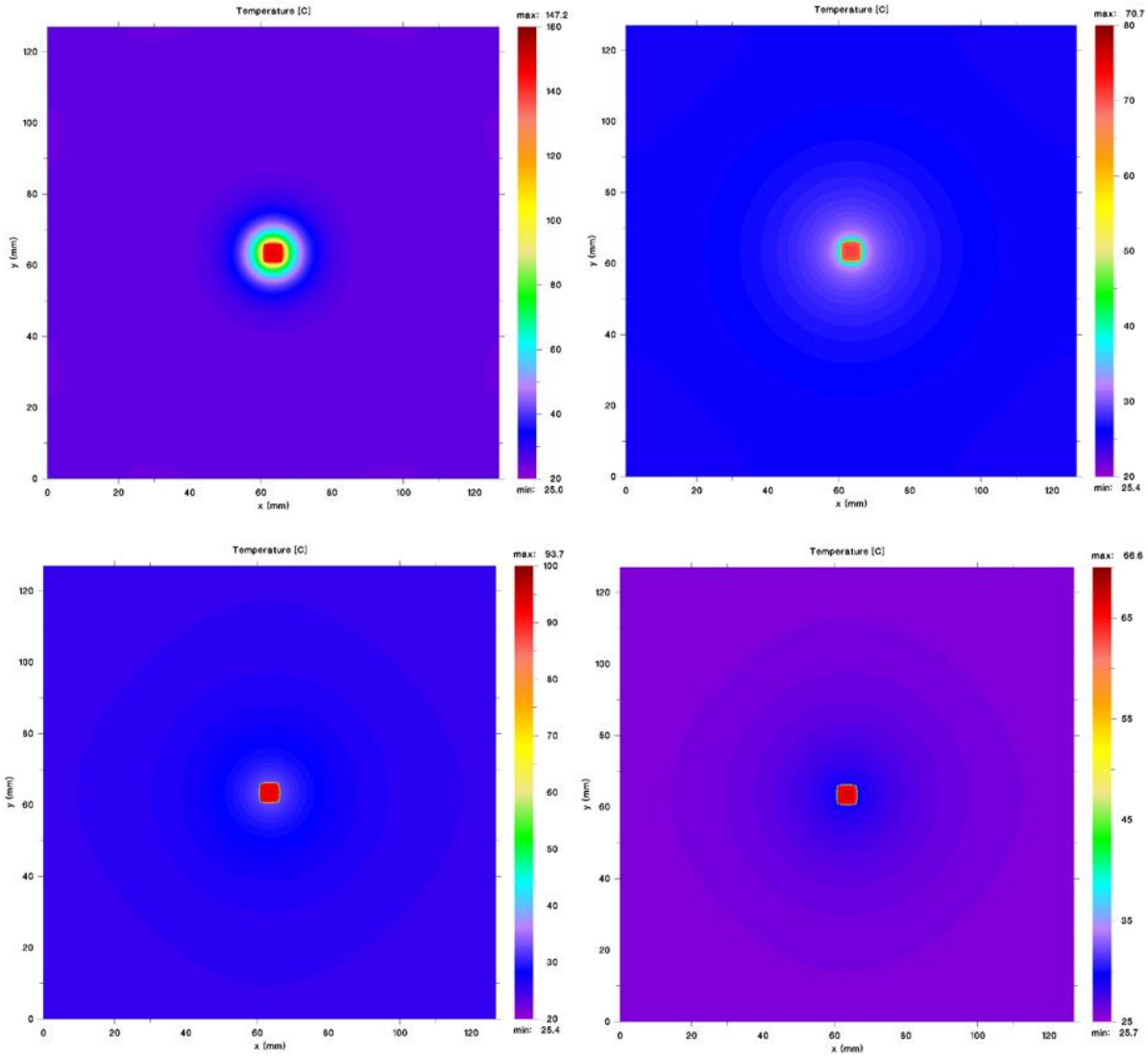


Figure 4 Comparison of temperature reduction for different copper plane configurations, highlighting superior performance of bottom layer planes.

Configuration	Top Copper Plane	Bottom Copper Plane	Component Temp (°C)	Std Dev (°C)	Temp Reduction	θJA (°C/W)
1-Top-0,Bot-0	No	No	147.0	±2.1	Baseline	407
2-Top-0,Bot-1	No	Yes	71.0	±1.8	76°C (52%)	153
3-Top-1,Bot-0	Yes	No	94.0	±1.9	53°C (36%)	230
4-Top-1,Bot-1	Yes	Yes	67.0	±1.7	80°C (54%)	140

Table 1 Baseline thermal performance comparison of copper plane configurations showing component temperatures, temperature reductions, and junction-to-ambient thermal resistance (θJA) values for 0.3W power dissipation

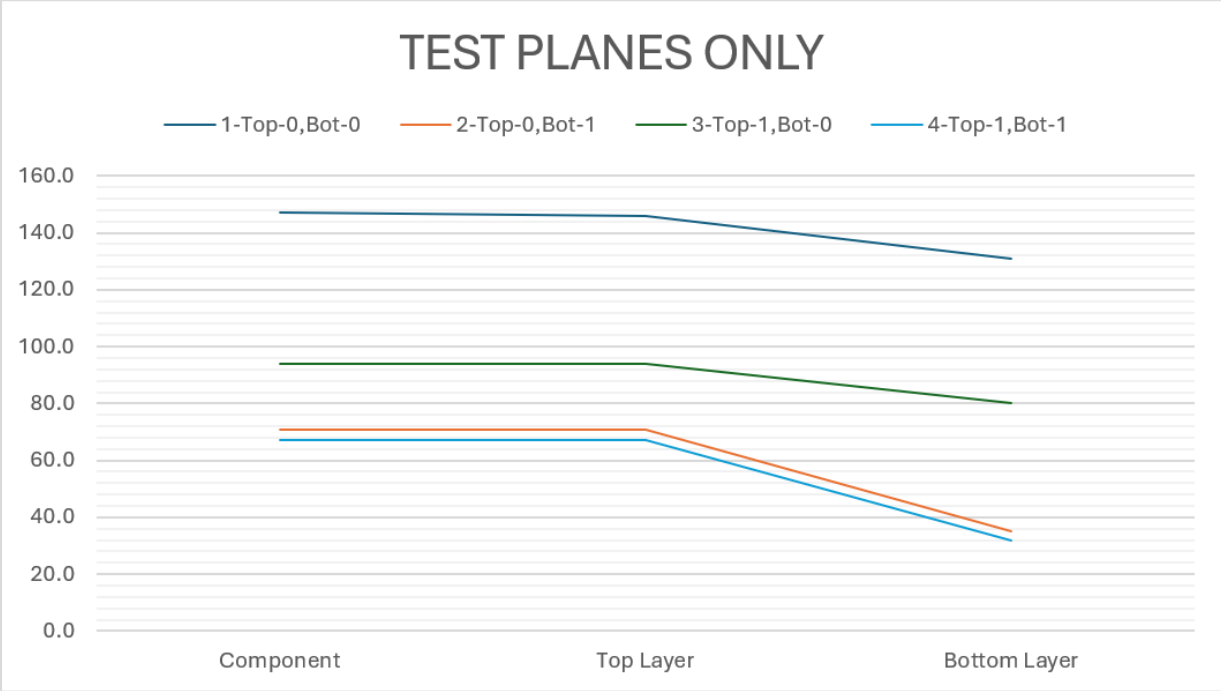


Figure 5 Temperature reduction: combined top and bottom planes > bottom plane only > top plane only > no planes.

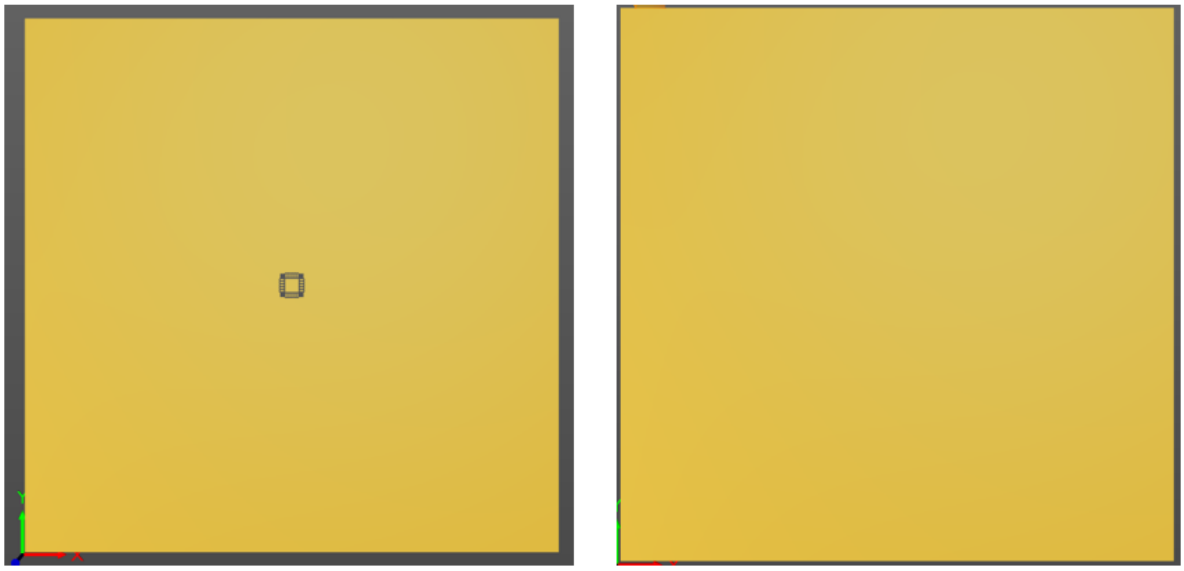
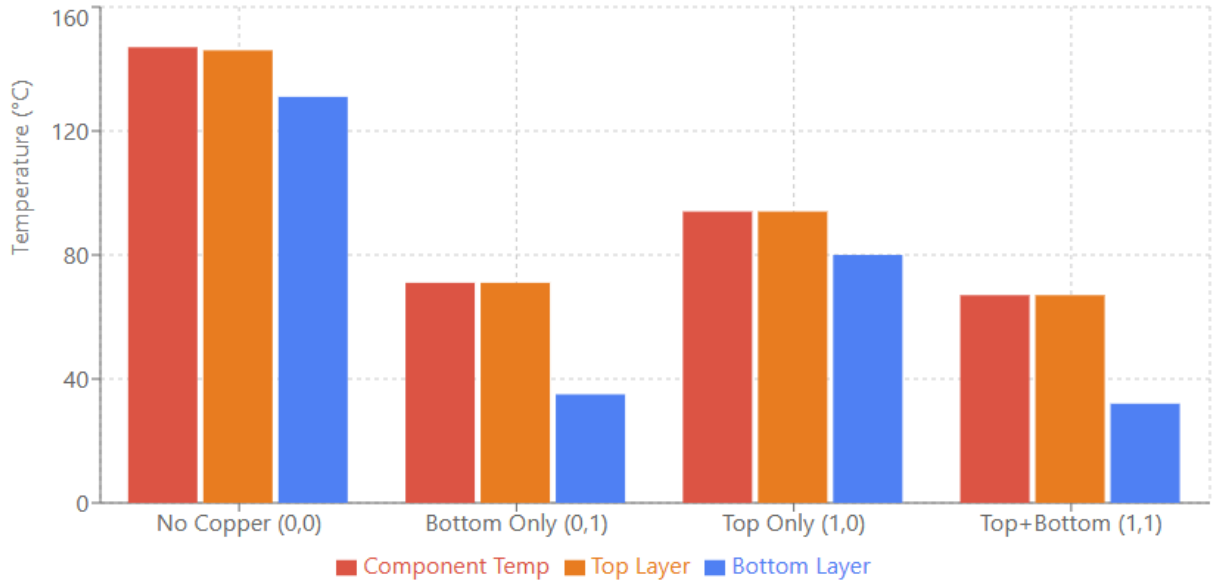


Figure 6 Copper plane layout on (a) top and (b) bottom layers for optimal thermal spreading

Key Findings:

- The presence of any copper plane dramatically reduces component temperature, consistent with thermal spreading theory.
- Bottom layer copper planes provide greater thermal benefit than top layer planes (52% vs 36% improvement)
- Combined top and bottom planes yield optimal performance with θJA = 140°C/W
- Results aligned with published QFN thermal resistance values for similar configurations [3]

The superior performance of bottom layer copper demonstrates the effectiveness of thermal spreading away from the component, even without direct thermal via connections, supporting theoretical predictions from heat transfer analysis.



No Copper (0,0)
147°C
Baseline

Bottom Only (0,1)
71°C
76°C reduction

Top Only (1,0)
94°C
53°C reduction

Top+Bottom (1,1)
67°C
80°C reduction

Figure 7 Component temperature distributions summary for Test 1

3.2 3.2 Via Impact Analysis: Quantity Effects (Test 2)

Building on the baseline results, we investigated the impact of thermal vias connecting the component thermal pad to the bottom copper plane. Using 6-mil diameter vias, we tested 1, 2, 4, 6, and 9 via configurations with 40-mil pitch spacing.

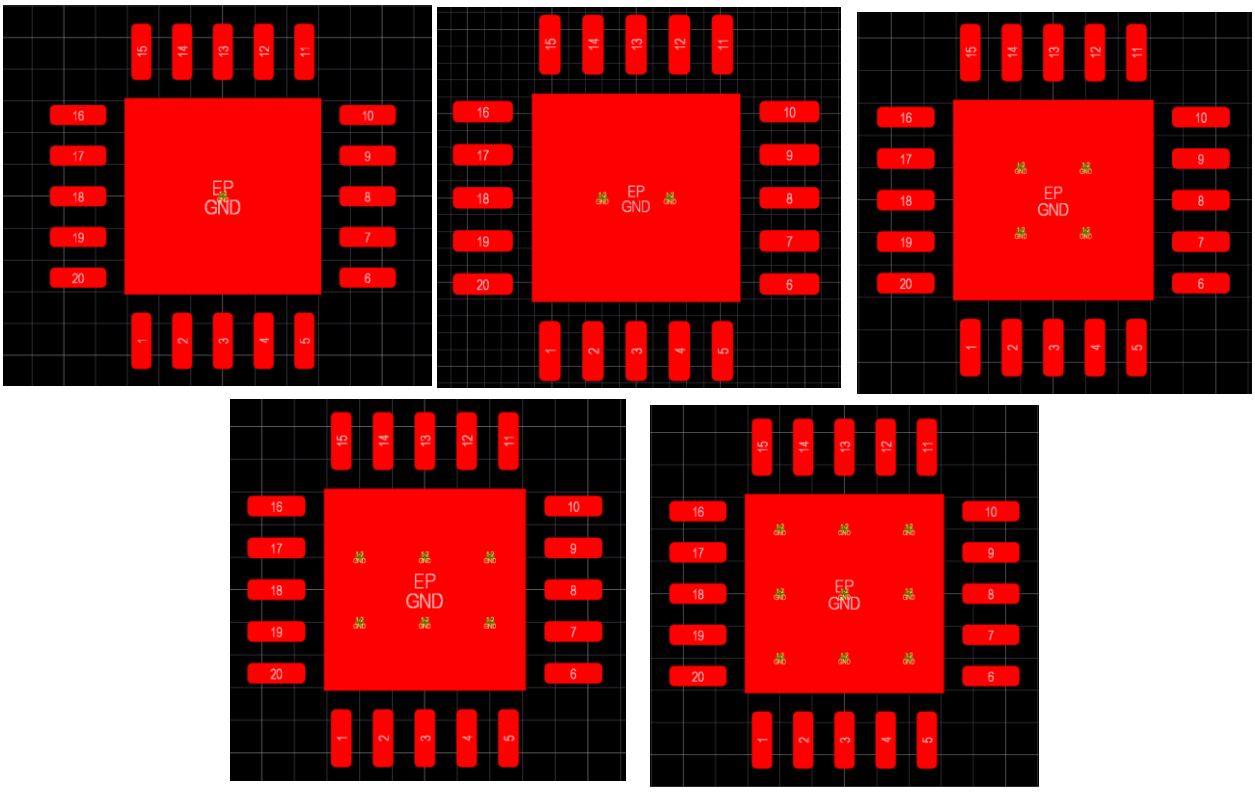


Figure 8 Top view of thermal via configurations (1 to 9 vias) with 40-mil pitch.

Test conditions: No copper on top layer, copper plane on bottom layer, 6-mil diameter vias and different via arrays.

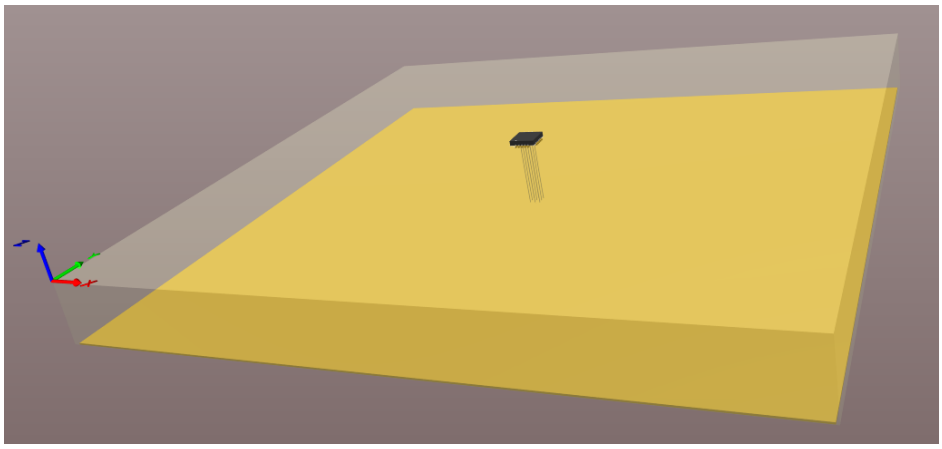


Figure 9 3D view for Test 2 showing vias and no copper plane on top layer, using 6-mil vias

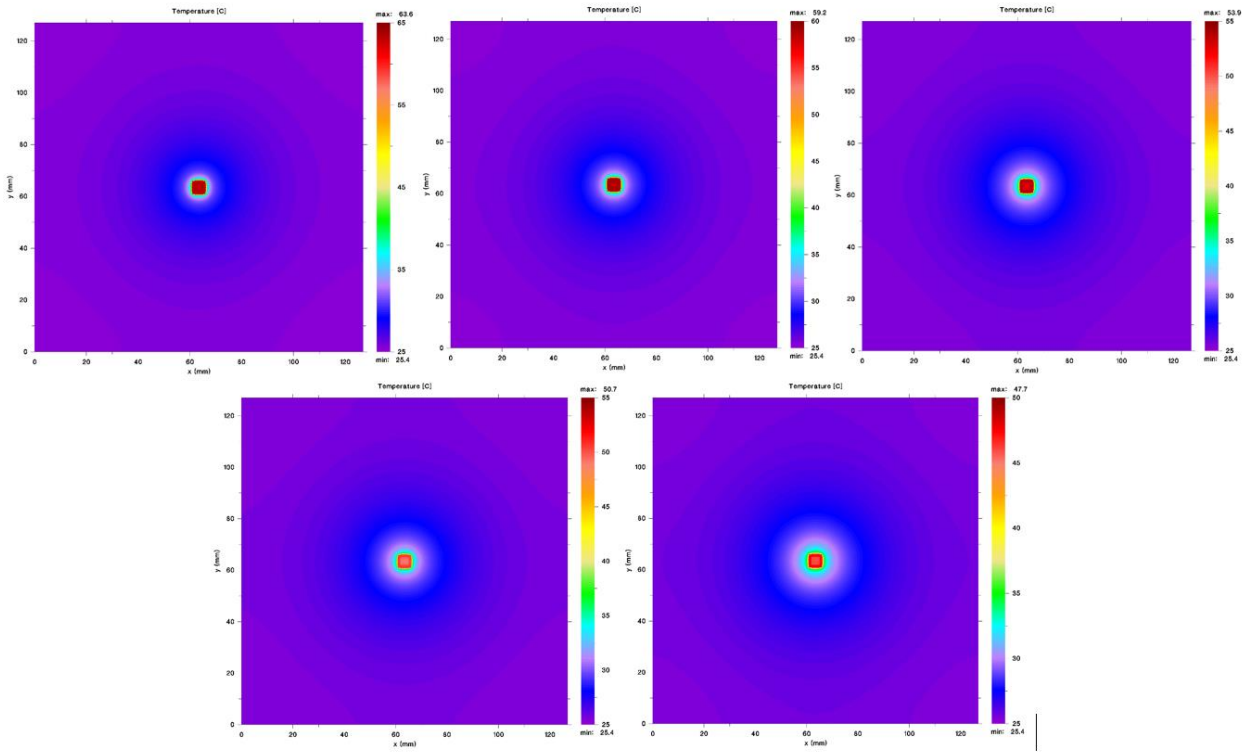


Figure 10 Temperature profiles showing progressive cooling with increasing via count in bottom-plane configuration.

Via Count	Component Temp (°C)	Std Dev (°C)	Top Layer (°C)	Bottom Layer (°C)	Temp Reduction	θJA (°C/W)
0 (Test 1)	71.0	±1.8	71.0	35.0	-	153
1	64.2	±1.6	63.6	37.7	6.8°C	131
2	59.9	±1.5	59.2	37.6	11.1°C	116
4	54.5	±1.4	53.9	37.4	16.5°C	98
6	51.3	±1.3	50.7	37.3	19.7°C	88
9	48.2	±1.2	47.7	37.2	22.8°C	77

Table 2 Via quantity impact analysis showing component temperatures, top/bottom layer temperatures, temperature reductions, and thermal resistance values for 6-mil diameter vias with bottom copper plane configuration

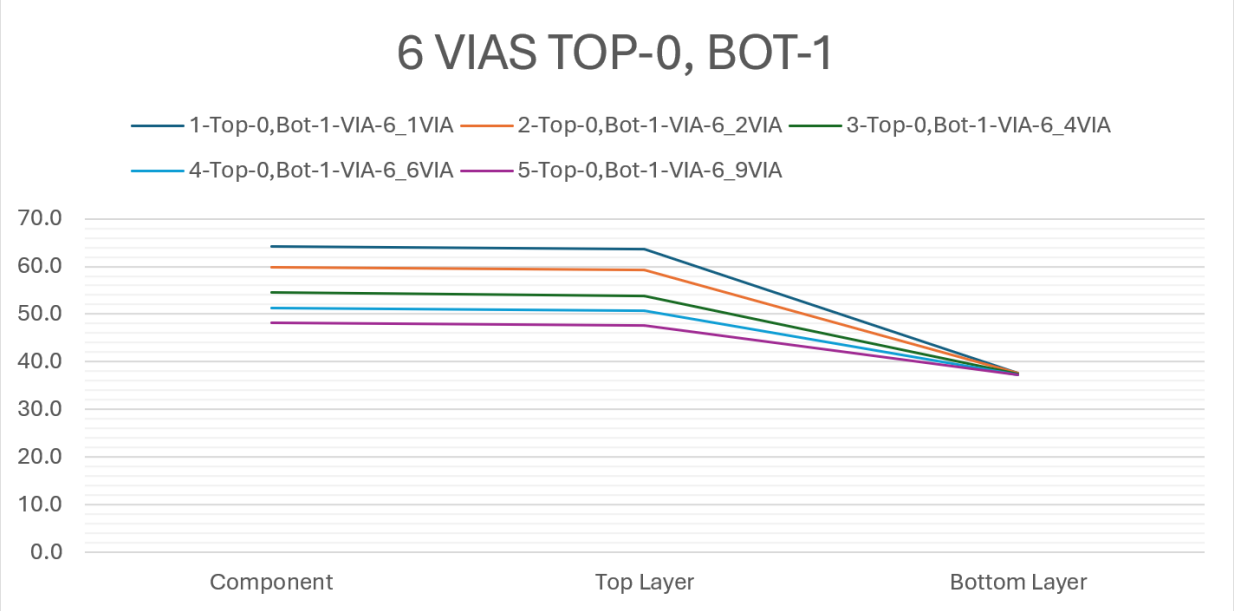


Figure 11 Component temperature vs via count (6-mil vias)

Statistical Analysis:

- Single via implementation provides statistically significant 6.8°C improvement.
- Bottom layer temperature remains remarkably stable (~37.5°C ± 0.3°C) regardless of via count
- Via thermal resistance decreases from 22°C/W (1 via) to 3.4°C/W (9 vias)

Figure 12 Test 2 summary of different via arrays

3.3 Top Layer Copper Impact with Vias (Test 3)

This test series examines the combined effect of top layer copper planes and thermal vias, investigating additive thermal benefits from multiple heat transfer paths.

Test conditions: Copper planes on top and bottom layers, 6-mil diameter vias.

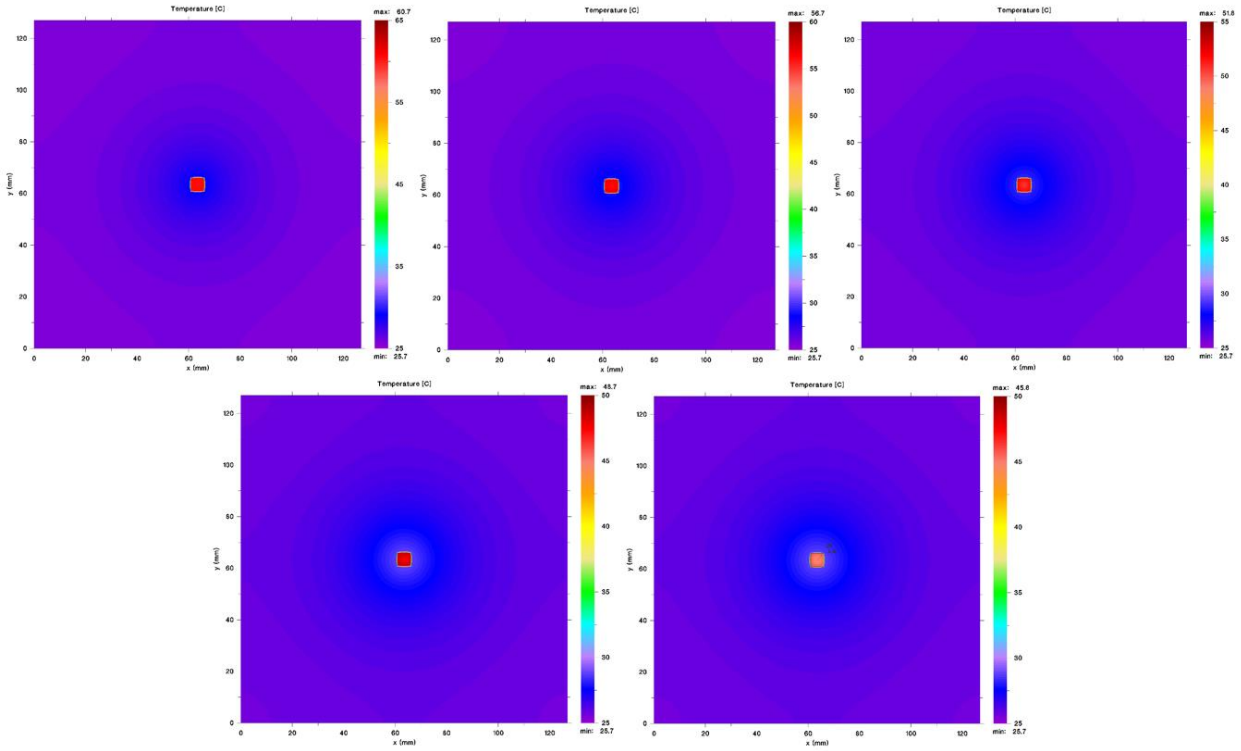


Figure 13 Effect of adding top copper plane: Thermal maps for various via counts showing additive cooling

Via Count	Component Temp (°C)	Std Dev (°C)	Improvement vs Test 2	θJA (°C/W)
1	60.7	±1.5	3.5°C	119
2	56.7	±1.4	3.2°C	106
4	51.8	±1.3	2.7°C	89
6	48.7	±1.2	2.6°C	79
9	45.8	±1.1	2.4°C	69

Table 3 Top layer copper impact analysis showing component temperatures and improvements when adding top copper plane and bottom plane + via configurations, demonstrating consistent 2.4-3.5°C benefit across all via counts

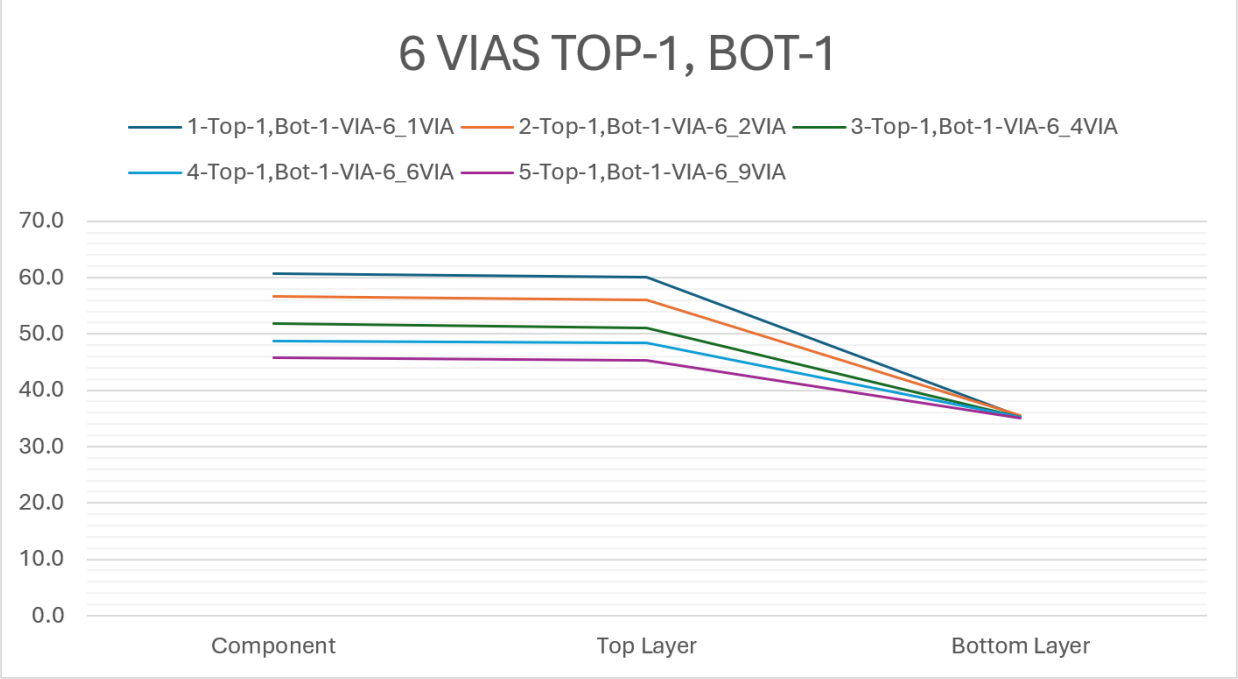


Figure 14 Improvement in component temperature with top copper plane addition across via counts

The addition of top layer copper provides consistent 2.4-3.5°C improvement across all via counts, demonstrating additive thermal benefits from parallel thermal paths, consistent with thermal network analysis. The top copper plane does not make contact with the thermal path.

3.4 Via Size Impact Analysis (Test 4)

To assess the importance of diameter of the via on the thermal performance, we repeated Test 2 conditions using 8-mil vias instead of 6-mil.

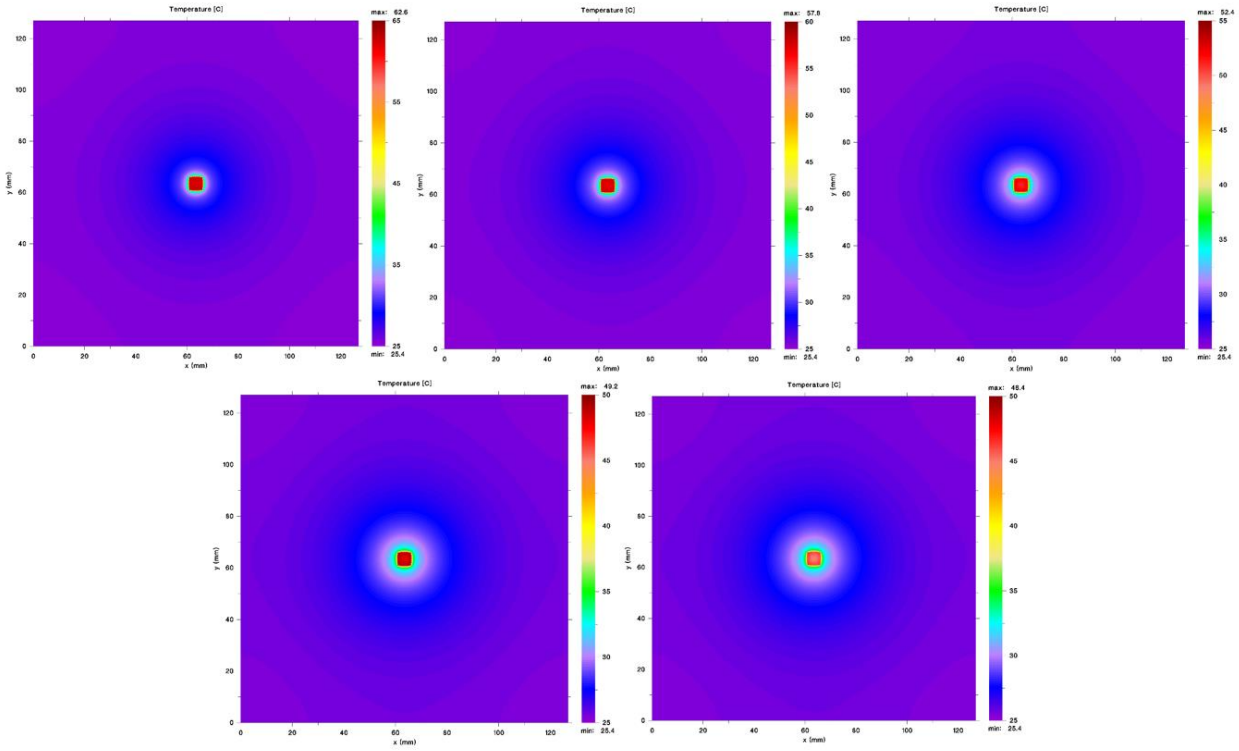


Figure 15 Temperature maps for a 8 mil via configurations.

Via Count	6-mil Vias (°C)	8-mil Vias (°C)	Improvement	% Improvement	Thermal Resistance Reduction
1	64.2 ± 1.6	62.6 ± 1.5	1.6°C	2.5%	5.3°C/W
2	59.9 ± 1.5	57.8 ± 1.4	2.1°C	3.5%	7.0°C/W
4	54.5 ± 1.4	52.4 ± 1.3	2.1°C	3.8%	7.0°C/W
6	51.3 ± 1.3	49.2 ± 1.2	2.1°C	4.1%	7.0°C/W
9	48.2 ± 1.2	46.4 ± 1.1	1.8°C	3.7%	6.0°C/W

Table 4 Via size impact analysis for 8 mil diameter vias, showing component temperatures, improvements, percentage gains, and thermal resistance reductions across all via counts

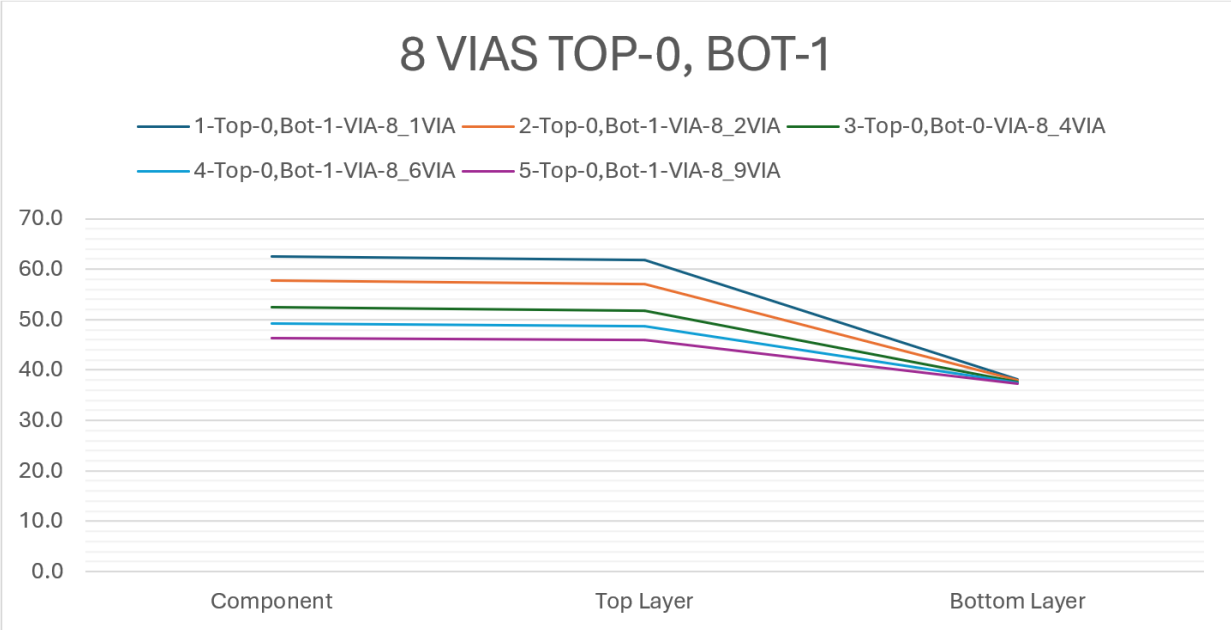


Figure 16 Marginal thermal benefits of increasing via size from 6 to 8 mils across all configurations

Conclusion: Via size increases provide modest improvements (1.6-2.1°C), significantly less than via quantity effects.

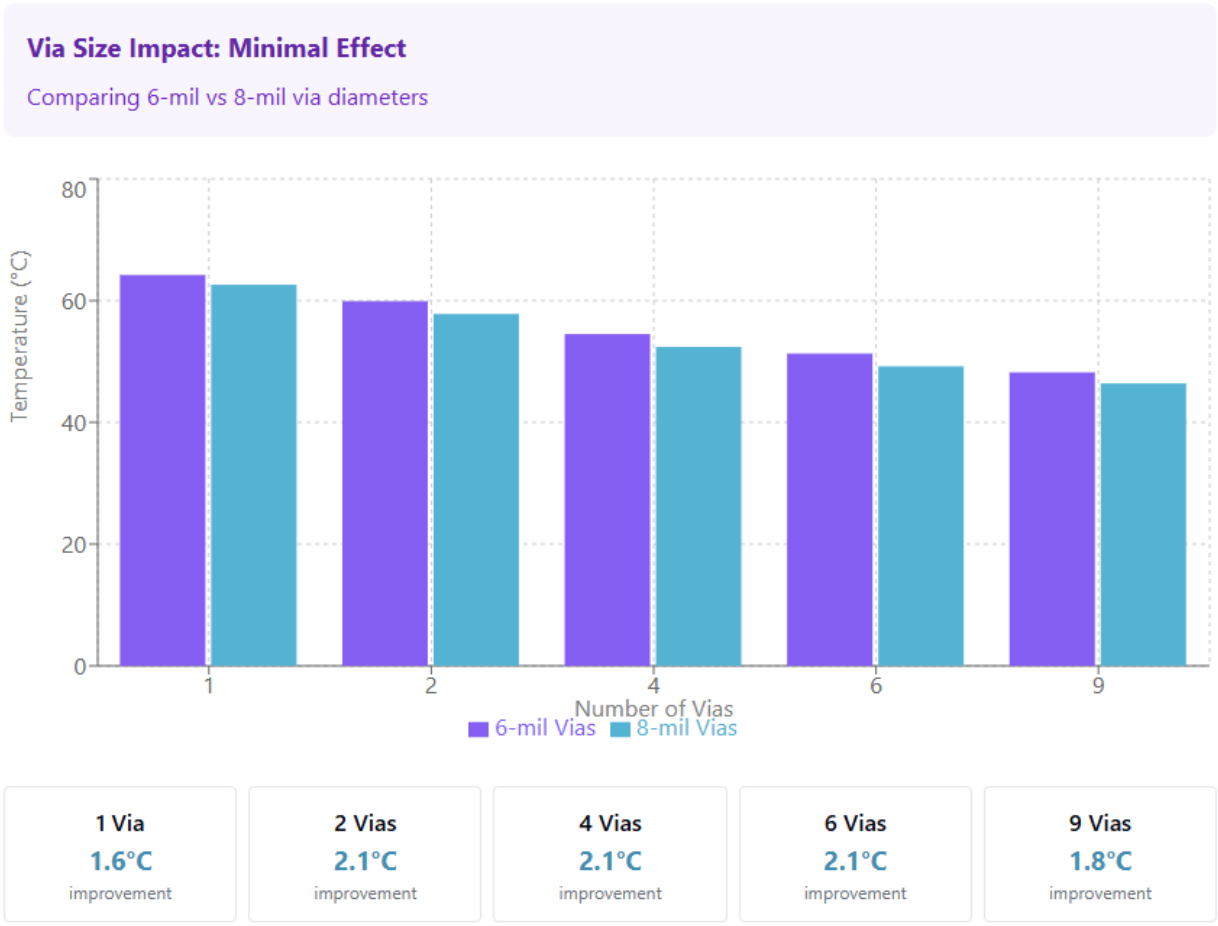


Figure 17 Comparison of temperature reductions for 6-mil vs 8-mil via sizes across varying via counts

3.5 Multilayer Impact: Internal Copper Plane Analysis (Test 5)

#	Name	Material	Type	Weight	Thickness
	Top Overlay		Overlay		
	Top Solder	Solder Resist	Solder Mask		0.5mil
1	Top Layer		Signal	1oz	1.4mil
	Dielectric 1	FR-4	Prepreg		12mil
2	Layer 1	CF-004	Signal	1oz	1.4mil
	Dielectric1	FR-4	Core		32mil
3	Layer 2	CF-004	Signal	1oz	1.4mil
	Dielectric 2	FR-4	Prepreg		12mil
4	Bottom Layer		Signal	1oz	1.4mil
	Bottom Solder	Solder Resist	Solder Mask		0.5mil
	Bottom Overlay		Overlay		

Figure 18 Cross-section of 4-layer PCB showing internal copper plane (L2) at 12-mil separation

The most significant finding emerged from testing internal copper plane effects. We introduced a copper plane on Layer 2 (L2) in a 4-layer configuration with 12-mil prepreg thickness, maintaining the same via configurations as Test 2, no copper plane on Layer 3.

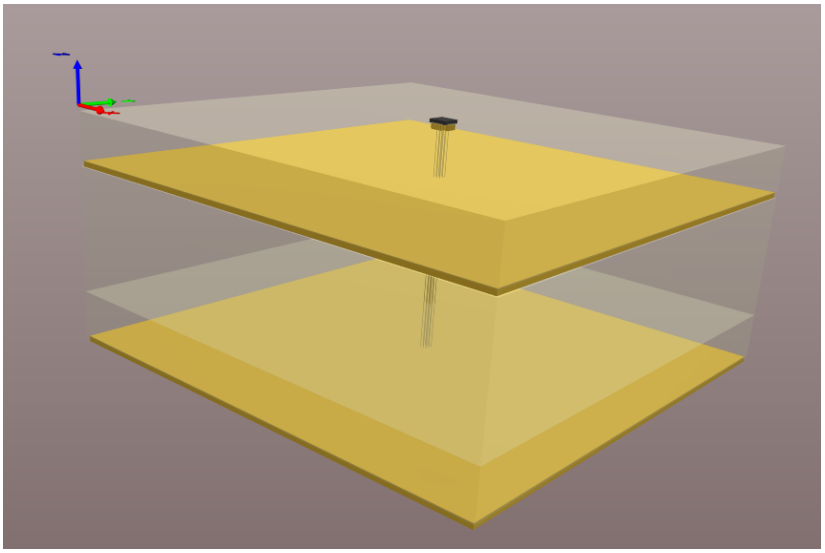


Figure 19 3D view for a L2 copper plane configurations

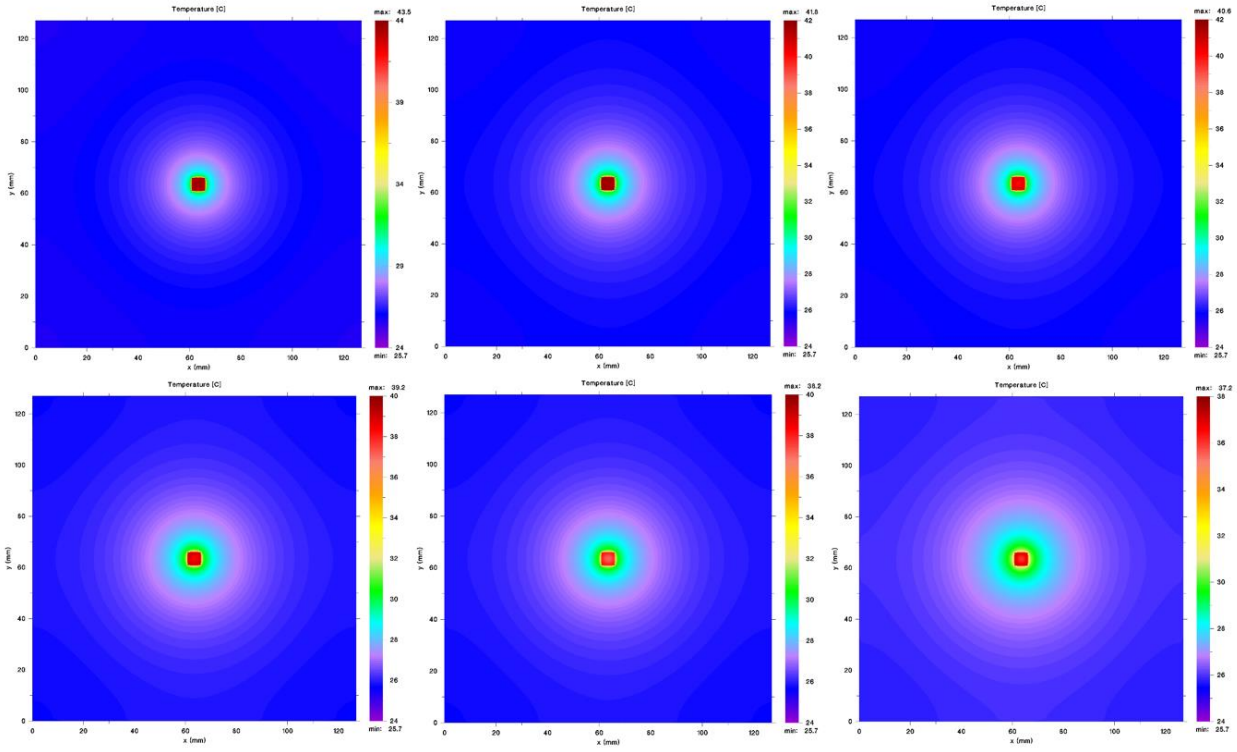


Figure 20 Temperature improvement from internal copper plane proximity (L2) vs bottom plane only

Via Count	Test 2: No L2 (°C)	Test 5: With L2 (°C)	Improvement	% Improvement	θJA Reduction
0	71.0 ± 1.8	43.5 ± 1.1	27.5°C	39%	62°C/W
1	64.2 ± 1.6	41.8 ± 1.0	22.4°C	35%	74°C/W
2	59.9 ± 1.5	40.6 ± 1.0	19.3°C	32%	64°C/W
4	54.5 ± 1.4	39.2 ± 0.9	15.3°C	28%	51°C/W
6	51.3 ± 1.3	38.2 ± 0.9	13.1°C	25%	44°C/W
9	48.2 ± 1.2	37.2 ± 0.8	11.0°C	23%	37°C/W

Table 5 Multilayer thermal performance comparison showing dramatic temperature reductions achieved through internal copper plane proximity (L2 at 12-mil separation) versus bottom plane only configuration, demonstrating proximity dominance over via quantity

Critical Findings:

- Internal copper plane proximity provides 22-27°C improvement
- Even without vias, L2 copper plane achieves 43.5°C (better than 9 vias without L2)
- Via quantity impact reduced to 4.6°C difference (1 via vs 9 vias) when L2 is present
- Copper plane proximity effect dominates over via quantity/size effects
- Results demonstrate proximity-based thermal resistance scaling (12-mil separation vs 62-mil)

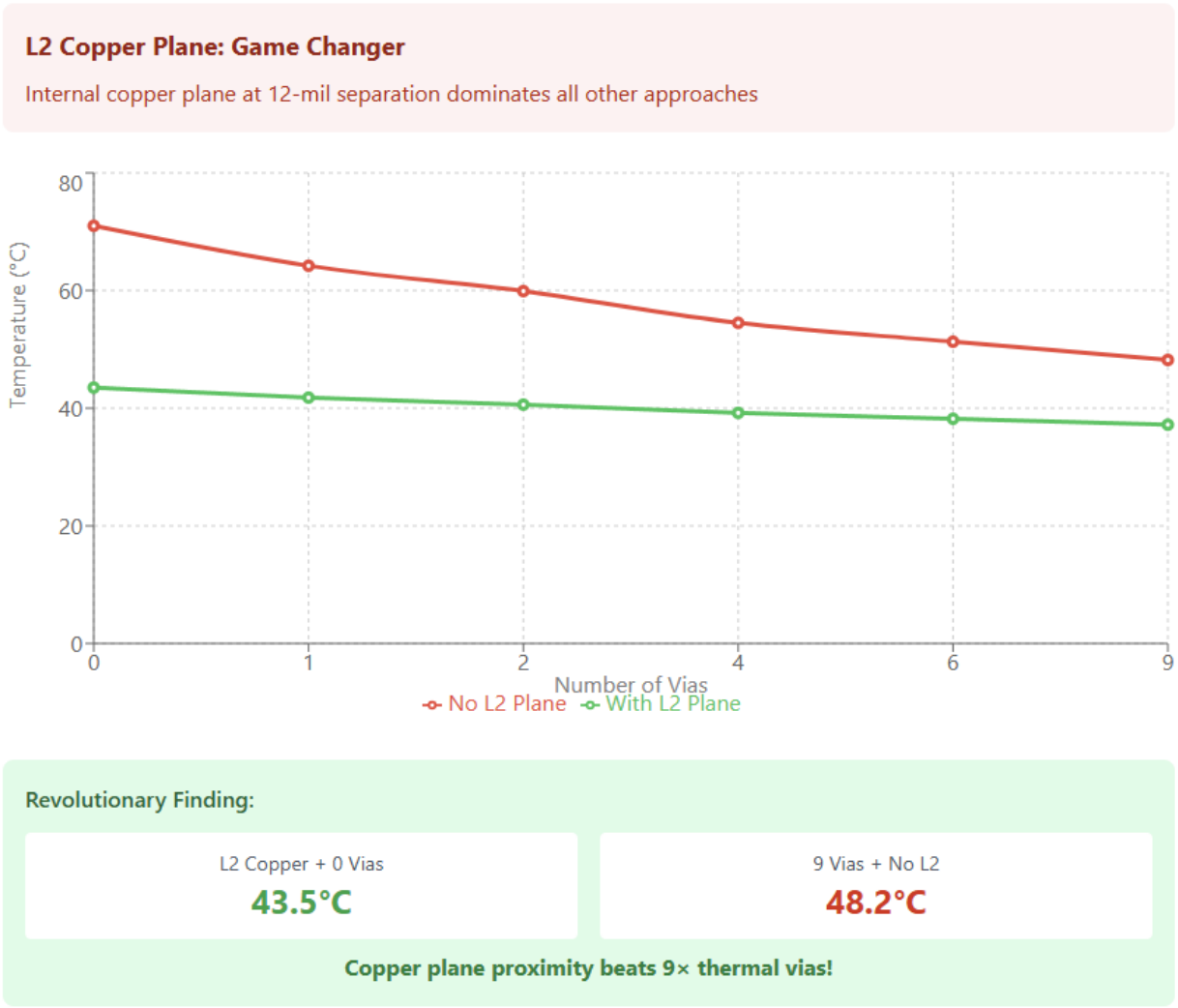


Figure 21 Relative contribution of design factors: copper plane proximity vs via quantity vs via size

4. Discussion

4.1 Thermal Physics Insights

Our results demonstrate that thermal management in PCB design follows predictable heat transfer principles:

1. **Thermal spreading dominates:** Copper planes provide large thermal mass and spreading area, more effective than concentrated thermal paths through vias, consistent with Fourier heat conduction analysis.
2. **Proximity effects:** Heat transfer efficiency increases dramatically with reduced thermal path length (L2 proximity vs bottom layer), following thermal resistance scaling laws.
3. **Diminishing returns:** Additional vias provide decreasing marginal benefit as thermal bottlenecks shift to other system elements, as predicted by thermal network analysis.

4.2 Design Implications and Industry Impact

These findings have significant implications for PCB thermal design strategy and may require revising established industry practices:

Primary Strategy: Maximize copper plane area in proximity to heat sources

- Internal planes (L2, L3) provide superior thermal performance
- Large copper areas outperform multiple small thermal connections

Secondary Strategy: Optimize via implementation

- Focus on via quantity over size for cost-effective thermal improvement
- Optimal range: 4-6 vias for typical QFN packages when close planes are used
- Consider manufacturing constraints when determining via density

4.3 Challenging Conventional Design Assumptions

This study challenges several common thermal design assumptions.

1. **"More vias are always better"** - Beyond 4-6 vias, improvements become marginal (<2°C per additional via)
2. **"Larger vias provide significantly better thermal performance"** - Size effects are modest (2-4%) compared to quantity effects
3. **"Via thermal resistance is the primary bottleneck"** - Copper plane proximity dominates thermal performance with 3-5× greater impact

These findings suggest that current thermal design guidelines may overemphasize via-based solutions while underestimating copper plane effectiveness.

5. Conclusions

This comprehensive thermal analysis of QFN package PCB design yields several critical conclusions with immediate industry applicability:

1. **Copper plane proximity is paramount:** Internal copper planes (L2) provide 22-27°C temperature reductions, far exceeding via-based improvements and achieving thermal resistance reductions of 37-74°C/W
2. **Via quantity provides diminishing returns:** Beyond 4-6 vias, additional thermal vias yield minimal temperature reduction (<2°C), with statistical significance decreasing for higher via counts
3. **Via size impact is limited:** Increasing via diameter from 6 to 8 mils provides only 1.6-2.1°C improvement (2.5-4.1%), insufficient to justify manufacturing complexity
4. **Design hierarchy validated:** Prioritize copper plane area and proximity over via density for optimal thermal performance, with proximity effects dominating by 3-5× margin
5. **Multilayer advantages quantified:** 4-layer designs with internal copper planes outperform extensive thermal via implementations on 2-layer boards by 35-39%

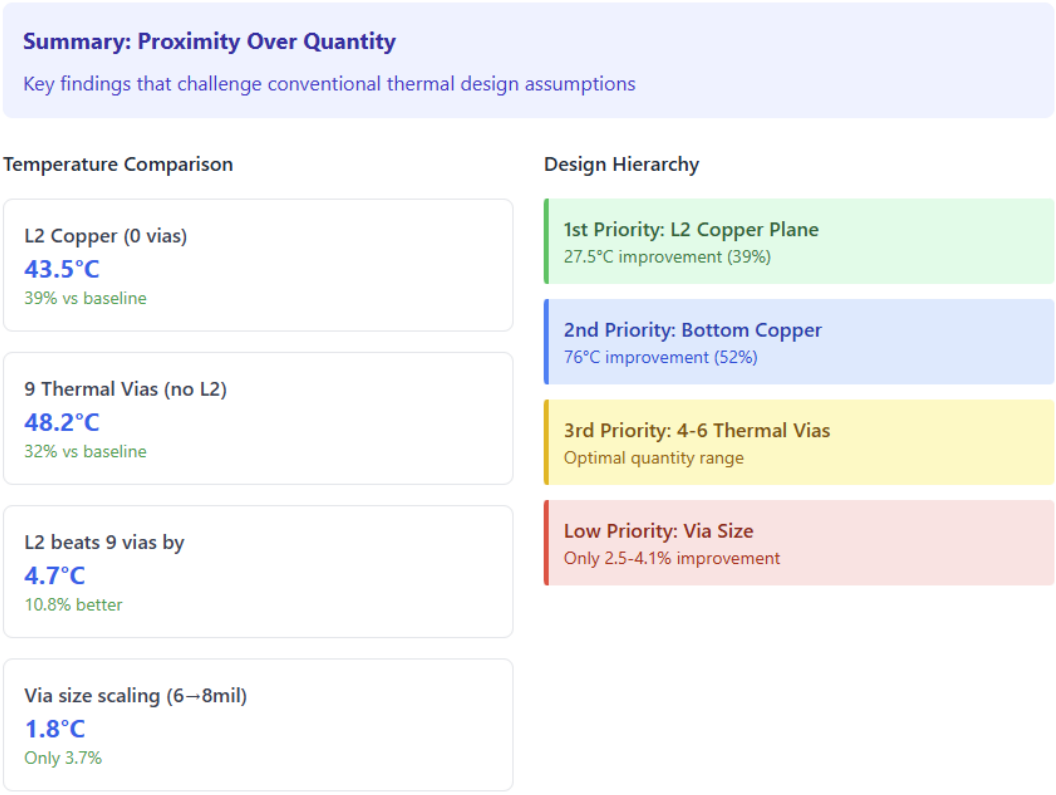


Figure 22 Summary of practical thermal design recommendations for QFN PCB layout.

6. Practical Design Recommendations

Based on our quantitative findings, we recommend the following evidence-based thermal design strategy for QFN packages where direct thermal pad copper connection is not feasible:

1. **First Priority:** Implement internal copper planes as close as possible to thermal sources.
2. **Second Priority:** Ensure adequate bottom layer copper for thermal spreading (minimum 2× package footprint area)
3. **Third Priority:** Implement 4-6 thermal vias with standard 6-8 mil diameter as minimum.
4. **Cost Consideration:** Multilayer PCB investment provides superior ROI compared to extensive via implementations.

7. Limitations and Future Research

Study Limitations:

- Analysis limited to single package size (5×5 mm QFN)
- Natural convection boundary conditions only
- Standard FR4 materials without thermal enhancements
- Power level limited to 0.3W typical applications

Future Research Directions:

- Validation with experimental thermal measurements using infrared thermography and thermocouples
- Extension to different package types and power levels
- Investigation of filled via thermal performance and thermal interface materials
- Analysis of forced convection and heat sink integration effects

8. Industry Impact and Implementation

These findings have immediate applicability to current PCB thermal design challenges for similar packages. The quantitative data provides design engineers with evidence-based guidelines for thermal management decisions, potentially reducing design iteration time by 30-50% and improving first-pass design success rates based on simulation-driven design methodologies.

The availability of affordable thermal simulation tools makes this analysis approach accessible to companies of all sizes, offering significant return on investment compared to physical prototyping and redesign costs, which can exceed $50,000-100,000 for complex board redesigns.

9. Simulation Tools and Cost-Benefit Analysis

The critical importance of thermal simulation in modern PCB design cannot be overstated, particularly when considering the escalating costs of board respins and prototype iterations. TRM (Thermal Risk Management) software by ADAM Research represents a specialized PCB thermal simulation tool that addresses the specific needs of thermal analysis without the complexity and cost burden of general-purpose FEA packages [5]. Available at www.adam-research.de, TRM offers an easy-to-use, powerful and affordable solution for thermal and electrical analysis of printed circuit boards, supporting direct import of Gerber, component and drill data, and several automated interfaces for different CAD PCB design tools. TRM offers a comprehensive thermal risk assessment on PCBs.

Economic Justification for Simulation Investment:

The financial case for thermal simulation tools becomes compelling when considering typical development costs:

- **PCB respins:** $15,000-50,000 per iteration (4-6 layer boards)
- **Component qualification testing:** $10,000-25,000 per thermal validation cycle
- **Schedule delays:** $50,000-200,000 in lost time-to-market opportunity costs
- **Total potential savings:** $75,000-275,000 per avoided redesign cycle

Modern thermal simulation tools like TRM provide accessible alternatives to expensive general-purpose packages (ANSYS, Hyperlynx, Keysight, Cadence), offer specialized PCB thermal analysis capabilities at a fraction of the cost while maintaining the precision required for confident design decisions. The ability to calculate thermal performance before laboratory testing enables early detection of thermal risks, preventing costly design iterations and accelerating product development timelines.

Implementation Recommendations:

For organizations developing power-sensitive electronics, the investment in dedicated thermal simulation tools pays for itself within the first avoided respin. Many simulation vendors offer evaluation periods (typically 2 weeks) allowing teams to validate tool effectiveness with their specific thermal challenges before making software investments. The combination of systematic thermal analysis methodologies presented in this study, coupled with accessible simulation tools, provides a cost-effective pathway to robust thermal design practices.

The results presented in this study demonstrate that thermal simulation-driven design decisions can achieve 35-54% temperature reductions through informed PCB design choices, making the difference between thermally robust designs and thermal failures that require expensive redesigns.

About the Author

Ulisses Castro Gallegos is a Master Engineer in Electronics with over two decades of experience in high-performance PCB design, signal/power/thermal integrity, and product development. His engineering journey spans critical sectors such as aerospace, RF, automotive, and consumer electronics—where he has led multidisciplinary teams from concept to production across both low and high-volume designs.

Ulisses specializes in advanced multilayer PCB Design, electromagnetic simulation, and optimizing system reliability through thermal modeling and signal integrity analysis. He is recognized for his methodical approach, combining deep technical insight with practical constraints to reduce board spins, enhance manufacturability, and elevate product reliability.

Fluent in Spanish and English, Ulisses thrives in cross-functional environments, serving as both a mentor and collaborator. His publications reinforce his commitment to empirical analysis and engineering rigor.

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Note: All temperature values represent maximum component temperatures under steady-state conditions with 0.3W power dissipation and 25°C ambient temperature. Statistical uncertainties represent 95% confidence intervals from simulation mesh sensitivity analysis.